Application of Integrated Magnetics and Discontinuous Conduction Mode to Multi-port DC-DC Power Conversion for integrating PV panels with storage

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Abstract

Multi-port converter design and analysis presents one of the most intriguing challenges in the incorporation of renewables in the power grid. Choice of topology is of paramount importance to improve the power conditioning. To this effect, the Ćuk topology can be a suitable candidate : low Electromagnetic Interference (EMI), low component count, simplified Maximum Power Point Tracking (MPPT) and power management, reduction of filter capacitor requirement, high efficiency. This thesis revisits the concept of integrated magnetics in the Ćuk topology and uses it judiciously to achieve the aforementioned requirements, by generating ripple-free currents at two terminals, independent regulation of two outputs in addition to magnetic integration. However, till date, no completely deterministic method has existed to design the integrated magnetic version of the Ćuk converter. Two different methods, adopted from the area-product and the K_g (geometrical constant) methods are explored to design the two-port version of this converter. The area-product method is validated by means of experimental results on a 250W prototype. The ideas are then extended to a three-port version, but with the addition of another feature: independent regulation of two output ports. This is achieved by means of a combined Continuous Conduction Mode (CCM)-Discontinuous Conduction Mode (DCM) operation, but without sacrificing the ripple-free nature of currents on two of the ports. The non-isolated version of this converter, meant for modular use in a microconverter architecture, is validated by means of simulation and experimental results on a 150W prototype.

A soft-switching scheme has also been demonstrated for a three-port converter with integrated magnetics. This has an active-clamp Zero-Voltage Switching (ZVS) turn-on circuit with the addition of a Zero-Current Switching (ZCS) turn-off. The design of the external components and simulation results for the same are presented as well.

Finally, with the ever-increasing adoption of wide bandgap devices and planar magnetics in power electronics, it makes sense to get rid of the isolation transformer altogether for PV-to-grid applications, since isolation is not an imposed standard in PV power systems. Two Ćuk converter based topologies are proposed which are hybrid charge-pump/inductive converter circuits. Simulation results are presented for the same.

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Chapter 1

Introduction

Climate change is the gravest threat facing humanity [1]. Nearly 97 percent of the scientists believe that its caused by greenhouse gases due to human activities [2]. To combat this threat, two low-hanging fruits to generate electricity are the wind resource of 25-70 TWy/yr, and a three-orders of magnitude larger solar resource of 23,000 TWy/yr [3], both of which can also be used to electrify transportation [4].

For utilizing solar to generate electricity, without water-cooling required in concentrated solar plants [5], we have the following options: utility-scale solar, community-solar gardens and roof-top PVs. According to [6], the rooftop PV potential in the United States is 1,118 gigawatts of installed capacity and 1,432 terawatt-hours of annual energy generation, which equates to 39% of total national electric-sector sales, which is enormous. Given that residences already have a roof and thus dont require purchasing of land and all the associated regulatory and policy issues, the Master Plan, Part Deux [7]of Elon Musk to create stunning solar roofs with seamlessly integrated battery storage makes a great deal of sense combining PV panels and battery storage with roof shingles. The continuing drop in solar prices bode well for this trend [8].

Mortal Threat to Solar: However, there is a mortal threat to this promising solution. Utilities are looking at solar as detrimental to their survival for valid reasons. This has to do with the "duck curve" shown here [9] in Fig. 1.1. It shows that during midday when the PV generation peaks, the utilities have a large over-generation capacity, while they have to supply the peak power in the early evening hours when the demand is high, as people return home and the solar output declines. Also, the ramp rate is very significant projected in 2020 to be 14,000 MWs in just a few hours. Utilities

buy the peak power from low-efficiency power plants using single-cycle gas turbines at almost twice the cost compared to the revenue they get from customers. Therefore, the utilities face a double whammy losing revenue by not selling their product while having to maintain the infrastructure, and having to purchase electricity at much higher cost at peak hours. These peaking plants are also very inefficient, resulting in a great deal of GHG emissions.

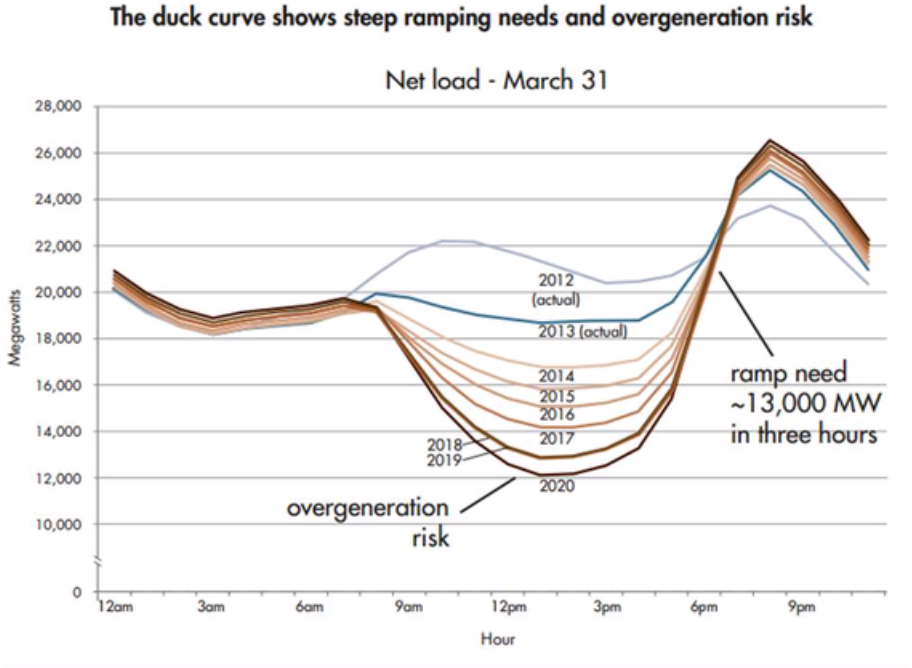

Figure 1.1: "Duck" Curve [9]

As a consequence, the states like Nevada have rolled back the clock on net metering and the PUC order tripled the fixed charges solar customers will pay over the next four years and reduced the credit solar customers receive for net excess generation by three-quarters [10]. As a consequence, most of the solar installers have left Nevada with job losses in thousands. A similar threat on a much larger scale may be looming in California and other states with much bigger potential for roof-top solar [11], where many utilities have rulings passed in their favor, similar to Nevada. Another concern has to do with the grid stability. Variable generation due to renewables such as solar can make the electric grid become unstable if a large amount of generation suddenly either comes-on or goes-off due to a fast-moving cloud cover, for example. A number

often mentioned is that up to 20 percent renewables is manageable but no more. Solar-friendly Germany, Europes champion for renewable energy, hoping to slow the burst of new renewable energy on its grid, has eliminated an open-ended subsidy for solar and wind power and put a ceiling on additional renewable capacity [12]. But if we are serious about combating climate change, we should dream of a much larger percentage perhaps 100 percent that is possible [13]. There are other pesky issues such as sudden change in output from solar, leading to rapid voltage fluctuations causing irritating light flicker. If not addressed, these problems may kill solar in its infancy.

Making the Case for Distributed Battery Storage: Batteries can store some of the peak energy generated during midday and supply it back during the early evening hours, thus leveling the load seen by the utilities. Thus the utilities will be able to use their base generation and avoid peaking units that are more expensive to use and more polluting. In doing so, the distributed battery storage has many advantages. This will result in less losses in transmitting electricity on the distribution network by having the energy available at the load site where its needed. Also, when the electricity is transmitted, the network is not highly loaded, avoiding a condition that results in higher power losses. By energy storage, the rate of change in the PV output can be reduced, leading to much higher than 20 percentage of renewables before the stability of the grid becomes an issue. Adding extra conventional capacitors or using super-capacitors [14] that allow fast charge/discharge, the problem of flicker can be mitigated. There is a great deal of ongoing research in batteries for automotive and grid applications [13] with significant room for potential advances. However, the topologies proposed in this thesis are agnostic of the battery type and should be able to deal with any battery charge/discharge characteristic.

1.1 Multi-port DC-DC power conversion

The Multi-Port Power Electronic Interface (MPEI) is shown in Fig. 1.2. The simultaneous requirements are that the PV should operate at their maximum power point at all times, the storage battery should be able to supply/sink power independently, and the utility port should have a large capacitor that is able to store energy for power-exchange with the utility.

Towards this objective, the dc-dc converter has three ports: 1) a PV-port, 2) a battery-port, and 3) the utility-port with large capacitance (or super-capacitors) to

supply the single-phase utility grid through a micro-inverter.

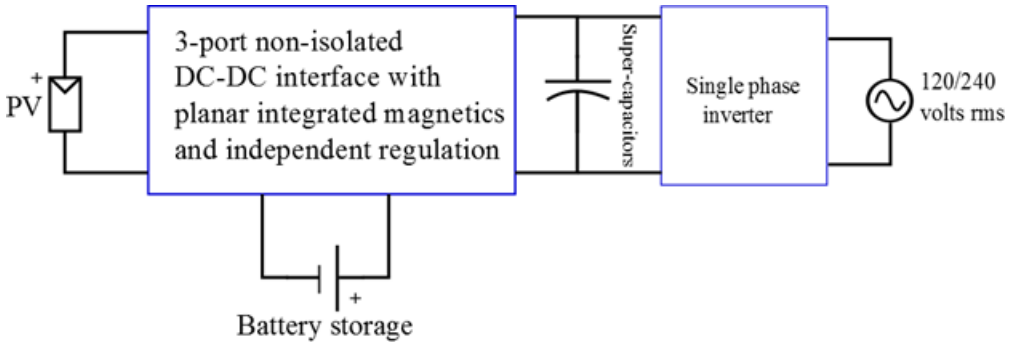

Figure 1.2: Integrated PV interface with storage

The unique characteristics of this interface are as follows: 1) The PV-port can maintain independently the PV output at the maximum power point (MPP), and the battery-port has the bidirectional power flow capability and can be independently control the desired charge/discharge rate of the battery; 2) The currents at the PV-port and the battery-port are almost ripple free (no need for extra filters); 3) The current at the utility-port is allowed to have a large ripple because of a large capacitor (or super-capacitors) have a large high-frequency current-carrying capability; 4) A high-frequency transformer may be part of this circuit, in that case the voltage across the capacitor at the utility-port can be much higher, e.g., the PV and the battery may be around 30 volts while the utility-port may be at 400 V to supply power into the single-phase utility through the micro-inverter; and 5) The voltage across the capacitor at the utility-port is allowed to vary a great deal while the interface is operating to mitigate flicker by rapid power transfer from the capacitor.

1.2 State-of-the-Art

There are many approaches to solving the multi-port problem for integrating renewables with storage. All of the existing topologies can be grouped into three main sub-divisions: non-isolated [15, 16, 17, 18, 19, 20], partially isolated [21, 22, 23, 24] and fully isolated [25, 26, 27, 28]. As far as three-port topologies are concerned, we will be evaluating [15, 16, 17, 18, 19, 20] since only those are relevant to the multi-port converter discussed in Chapter 6 of this thesis. In [15], a combination of three boost converters and one buck-boost converter was used on the input stage, which offered continuous current on

the PV side but did not eliminate the switching ripple. A three input boost converter was proposed in [16], which had switching ripple on the input current and multiple decentralized control loops. Reference [17] used a modified three-input buck-boost converter but required additional filtering components. Also, it can only offer step-up dc-dc conversion. A family of non-isolated multiport topologies was proposed in [18], however, it uses competitive unified mode selection and independent control of some ports is lost. Wu et al.[19] describes an integrated three-port converter (TPC) which uses two active-clamp circuits to achieve converter control using the same duty ratios in two different modes. In [20], a modular multilevel approach is used for interfacing multiple sources and multiple loads, but there is no concept of a storage port. The topologies described thus far did not use integrated magnetics.

1.3 Outline and Contributions of the Thesis

1.3.1 A Systematic Design Method and Verification of a Zero Current Ripple Interface for PV-to-Battery Applications

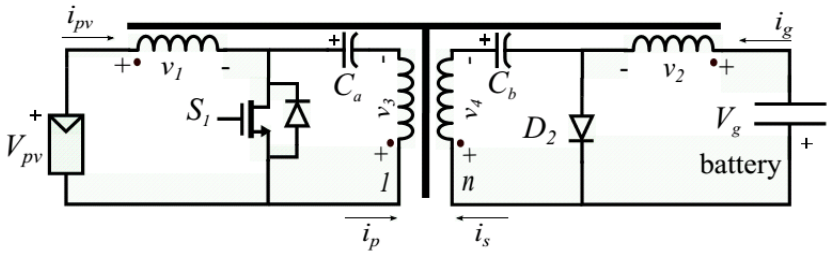

Figure 1.3: PV-to-Battery Interface

A systematic method of designing a zero terminal current ripple integrated magnetic Ćuk converter for Photovoltaic (PV)-to-Battery applications is presented in this section. This converter is shown in Fig. 1.3. The four winding coupled inductor design consists of two inductors and a two-winding transformer coupled on a common EE-core. The core design uses a simplified flux-reluctance model to arrive at the Area Product formulation for this kind of four winding structure. The zero-ripple condition in the terminal currents is achieved by controlling the coupling coefficients by means of air-gap reluctances in the core. Unlike the earlier designs for this converter, it provides a completely analytical approach to design this converter for a range of duty ratio. The

validity of the proposed method is confirmed using finite element analyses (both 2-D and 3-D), thermal validation and circuit simulations in PSpice. The zero-ripple condition is verified experimentally.

1.3.2 A Copper-loss Based Design Method and Verification for a Zero-ripple Interface for PV/Battery-to-Grid Applications

A systematic design of a zero-ripple Ćuk converter for PV/Battery-to-grid dc-dc conversion is presented. This work derives the copper loss geometrical constant (K_g) for this kind of integrated magnetic core using a simplified yet intuitive flux-reluctance model. Unlike earlier designs, the design procedure is completely analytical and valid for a range of duty-ratio operation. Verification is done by finite element methods and circuit simulations.

1.3.3 Active-Clamp Soft-Switching of a Three-Port Integrated Magnetic Ćuk converter

The proposed topology is shown in Fig. 1.4. A key objective is to investigate the tradeoff due to addition of snubber and soft-switching components against the basic design of integrated magnetic components. The motivation of adding the soft-switching components is explained. The active-clamp circuit with the addition of a switch and clamp capacitor achieves the ZVS turn of both the primary side switches. The passive snubber branch with the extra inductor and capacitor add a ZCS turn-off of the primary side switches. The various stages in the soft-switching process are explained. The design considerations for all these components are explained from a nominal set of specs: power, voltage conversion ratio, and nominal duty-ratio. Finally, the trade-offs due to addition of these extra components on the zero-ripple condition is then presented.

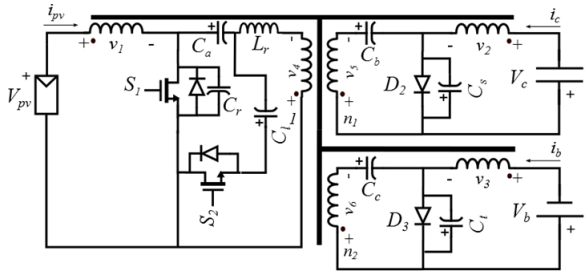

Figure 1.4: Soft-Switching 3-port Integrated Magnetic Ćuk Topology

1.3.4 A Modified Three-Port Ćuk Converter with Zero Ripple Terminal Currents on Two Ports and Independent Regulation of Output ports

A modified version of the three-port conventional Ćuk converter is discussed in this part of the thesis. The converter utilizes a three winding integrated magnetic structure on a EE-core for steering the ripple current of two terminals to a magnetizing inductance at the point of common coupling (PCC) of the two ports. The core design uses a simplified flux-reluctance model for an EE-core to arrive at the Area Product formulation for this structure. The zero-ripple condition in the two terminals is achieved by controlling the air-gap reluctances in the core. The converter uses a combination of continuous and discontinuous conduction modes to achieve independent voltage regulation of the two outputs. The target application is from interfacing solar PV with batteries and supercapacitors which can interface with a microinverter. The zero-ripple ports are designed to be PV and batteries which operate in Continuous Conduction Mode (CCM) and the third port (supercapacitor) operates in Discontinuous Conduction Mode (DCM). The setup is shown in Fig. 1.5. The validity of the proposed method is confirmed using circuit simulations in PSpice. The magnetics design process is supplemented with the help of finite-element modelling (FEM) calculations. The converter is bidirectional other than at the PV port. All the power flow modes are discussed in detail along with simulation and experimental results.

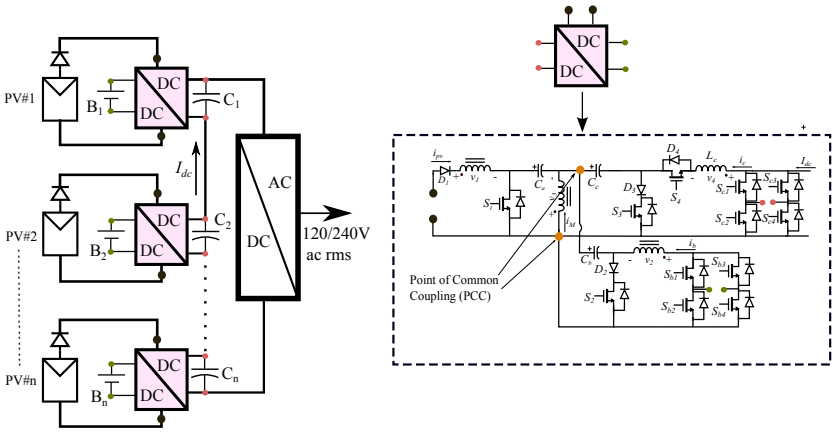

Figure 1.5: Application and Proposed Topology

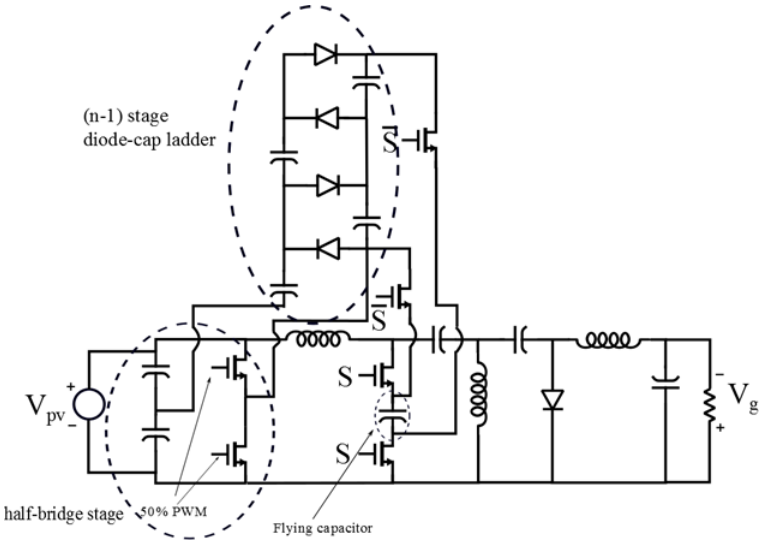

Figure 1.6: One of the High Step-up Transformerless Topologies Proposed in this Thesis

1.3.5 Transformerless High Step-up Hybrid Charge Pump Ćuk converter

In order to accelerate the adoption of solar PV, it is important for it to keep pace with the latest trends in power semiconductor devices and state-of-the-art passive design. This is accomplished by the use of wide-band gap devices and planar magnetics at very high switching frequencies ($>$ 500 kHz). This is usually a problem with topologies requiring transformer isolation, because it excites the interwinding capacitance in these magnetic devices at such high frequencies. On the other hand, it is very difficult to get high conversion ratios ($>$3) with non-isolated dc-dc converters due to parasitic resistances [29].

A couple of topologies, a half-bridge (Fig. 1.6) and a full-bridge variant of a diode-capacitor ladder hybrid Ćuk converter are proposed to address this problem. The origin of this converter is from adding an extra term to the volt-second balance equation, as is explained in a later chapter. The comparisons with Middlebrook's topology [30], which is predominantly inductive in nature, are laid out, which show that the proposed topology has a lower switch count for sufficiently higher conversion ratios.

Chapter 2

Integrated Magnetics

2.1 Rationale

The basic principle of a two-winding transformer is : An ac voltage waveform on the primary winding induces a proportional voltage waveform on the secondary winding, on account of the same flux flowing in the core. The cause-and-effect can be reversed, i.e., when the voltage waveforms on two magnetic devices are the same, they can be coupled on to a single magnetic core as demonstrated in Fig.2.1. The advantages are twofold : size and weight reduction, as well as performance improvement, as will be demonstrated.

For example, consider the separate inductor windings in Figure 2.1. The positive polarity terminals on each winding are marked with a dot. We have

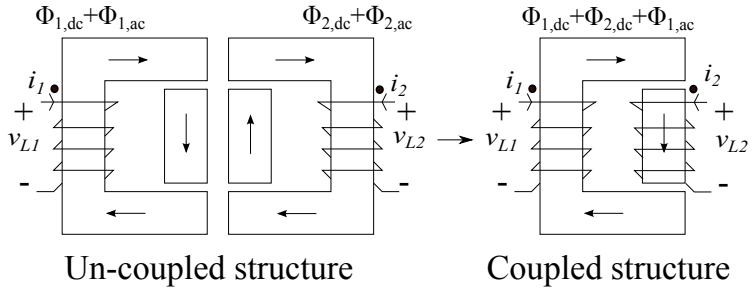

Figure 2.1: (a) Separate Inductors (b) Coupled Inductor Structure

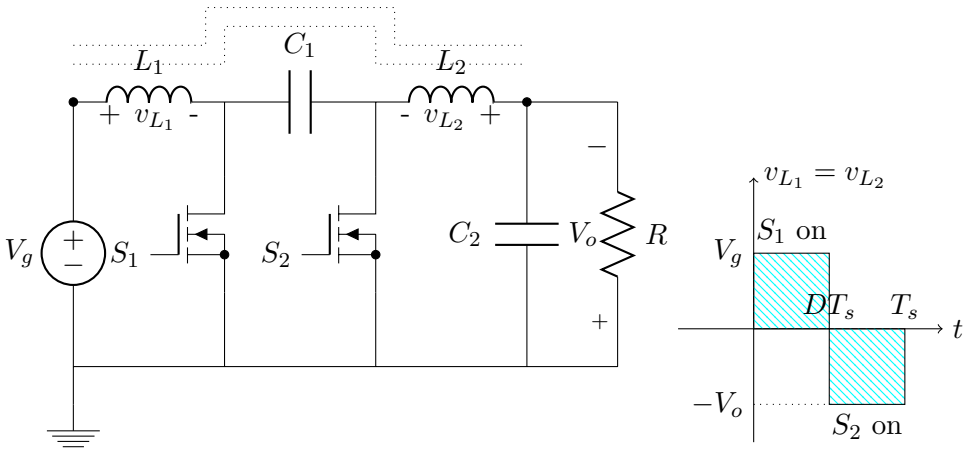

Figure 2.2: Basic Ćuk converter

$$\int v_{L_1} dt = \int v_{L_2} dt \tag{2.1}$$

$$\Delta\phi_{l_1} = \Delta\phi_{l_2} \tag{2.2}$$

Hence no ac flux flows through the center branch and it can be eliminated. The dc fluxes add up, according to the principle of superposition. However, the air-gap needs to be increased in order to maintain this linearity.

For the basic Ćuk converter (Fig. 2.2), it has this fortunate property of identical voltage waveforms across the inductors. Hence the total ac flux in the center branch (in Fig. 2.1) is zero, and can be removed. This leads to a smaller, lighter magnetic component but with the same power density. This directly leads to removal of additional core losses, thereby increasing efficiency.

Magnetic Scaling Law

For a transformer, or coupled inductor with identical voltage waveforms, the maximum voltages that can be supported without saturation on the primary and secondary windings are :

$$V_1 = 4N_1 B_{max} S f_s \tag{2.3}$$

$$V_2 = 4N_2 B_{max} S f_s \tag{2.4}$$

where B_{max}=max. flux density in the core, S= cross-section, f_S= switching frequency, and N_1 and N_2 are the turns of each winding. Also the window area W of the two-winding core in Fig. 1 is fully utilized when

$$kW = \frac{N_1 I_1 + N_2 I_2}{J} \tag{2.5}$$

where k is the empirical fill factor of the windings, and J the current density, usually about 2-4 A/mm^2. Hence the power handling capacity of the magnetic structure is given by

$$P = VI \propto kWS \propto l^4 \Rightarrow V(vol.) \propto P^{3/4} \tag{2.6}$$

It is clear that the volume/weight of a magnetic device as a function of the linear dimension (l) goes up slower than the power handling capacity. Therefore, significant increase in power density can be obtained by integrating the magnetics structure. Apart from this, special converters (like Ćuk) with identical voltage waveforms can have the additional advantage of the ripple-steering effect, as explained in the next section.

2.2 Ripple-Steering Phenomenon

This is a very general result and can be applied to all switching converters where the coupled inductor technique can be practiced to advantage. This is an ac phenomenon and works even under no-load condition, barring non-idealities. For a 2-winding inductor, we have the following equations:

$$v_{L_1} = L_{11} \frac{di_1}{dt} + L_M \frac{di_2}{dt} \tag{2.7}$$

$$v_{L_2} = L_M \frac{di_1}{dt} + L_{22} \frac{di_2}{dt} \tag{2.8}$$

The equations can be rearranged as

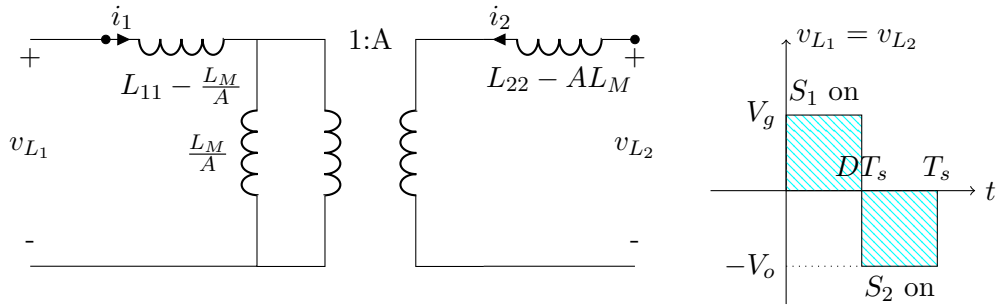

Figure 2.3: T-model of Coupled Inductor

$$v_{L_1} = (L_{11} - \frac{L_M}{A})\frac{di_1}{dt} + \frac{L_M}{A}\frac{d}{dt}(i_1 + Ai_2) \tag{2.9}$$

$$v_{L_2} = (L_{22} - AL_M)\frac{di_2}{dt} + AL_M\frac{d}{dt}(\frac{i_1}{A} + i_2) \tag{2.10}$$

Equations(2.9) and (2.10) mean the coupled inductor can be represented as the following 2-winding transformer (Fig. 2.3).

In order to have zero ripple current for the second winding, $\frac{di_2}{dt} = 0$. This happens when the voltage across $L_{22} - AL_M$ is zero. Solving the circuit (Fig. 2.3) gives

$$L_{11} = L_M \tag{2.11}$$

$$\Rightarrow n = k \tag{2.12}$$

where $n = \sqrt{L_{11}/L_{22}}$, $k = \frac{L_M}{\sqrt{L_{11}L_{22}}}$ (coupling coefficient)

Similar conditions can be derived for more complex magnetic structures. However, these design conditions are not practically very useful. A more physical, yet deterministic method is discussed in the next chapter for the 2-port integrated magnetic Ćuk converter.

Chapter 3

Two-Port Integrated Magnetic Ćuk converter for PV-to-Battery Applications

3.1 Introduction

DC-DC converters for interfacing PV panels to batteries are a topic of interest due to the growing interest in harvesting and storing energy from renewable sources. The main requirements of a converter in such an application include a wide conversion range (step-up/step-down), isolation to mitigate ground leakage currents [31, 32] and low terminal electromagnetic interference (EMI) [31, 32]. The boost converter is usually the topology of choice for simplicity of operation [33, 34, 16]. The Single-Ended-Primary-Inductor-Converter (SEPIC) is also used in certain cases [35], however it offers low ripple only on one terminal just like the boost. Resonant topologies [36] have also been proposed. However, the problem of EMI in power converters, as alluded to in [33, 34] can be addressed better by the isolated Ćuk converter [37]. Other applications include dc back-up energy systems for uninterruptible power supplies (UPS), high-intensity discharge lamps for automobiles, and the telecommunications industry [38, 39, 40], brushless DC drives [41].

The integrated magnetic isolated Ćuk converter proposed here is primarily to be used as a front-end step-up DC-DC stage for charging a high voltage battery pack (100-400 V) from a PV panel, whose voltage ranges from 30-40 V (Fig. 3.1). Additionally,

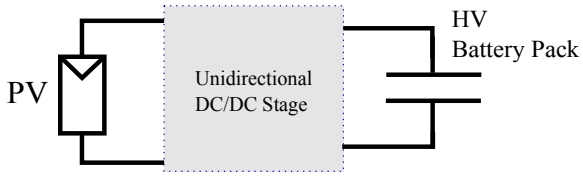

Figure 3.1: Application for the Ćuk converter

it can be a good candidate for solar automotive applications [42, 43]. Being a current-fed converter, it can interface with PV with relative ease. The galvanic isolation in the structure mitigates ground leakage currents. Finally, low ripple input and output currents mean that the PV capacitor requirement can be reduced, while nearly dc current is fed into the battery. The idea of this integrated magnetic converter is not novel in itself [37]. An analytical condition on the inductance matrix, as shown in Section II, can be derived which shows that the zero-ripple terminal current operation is theoretically possible. There are a few notable solutions to date [44, 45, 46, 47], but are mostly semi-analytical. For example, [44] has deficiencies in picking the area-product simply because the formulation does not have all known parameters and require initial estimates of certain inductances. In [45], the authors define a "leakage parameter", and provide a set of values of that parameter for a number of EE-cores. The treatment in [46, 47] is more circuit-oriented. However, this characterization requires a priori knowledge of the winding arrangement in addition to the core dimensions. Lack of a systematic method determining the power converter requirements into a viable magnetic design has prevented the integrated magnetic Ćuk converter from being used.

The content of this chapter first appeared in [48]. The following sections describe in more detail the design of this complex converter.

3.2 Description of the Converter

The converter schematic is shown in Fig. 3.2. Regarding the magnetics design for the converter, with the four-winding coupled inductor with windings designated by numbers in Fig. 3.2, we have the following set of equations:

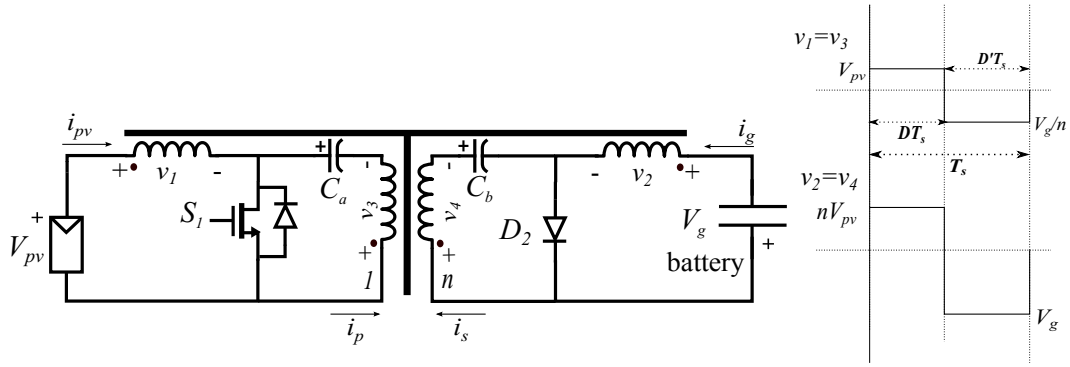

Figure 3.2: Integrated Magnetic Ćuk converter interface between PV panel and battery

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{12} & L_{22} & L_{23} & L_{24} \\ L_{13} & L_{23} & L_{33} & L_{34} \\ L_{14} & L_{24} & L_{34} & L_{44} \end{bmatrix} \times \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \tag{3.1}$$

where L_{jj} = self-inductance of j^{th} winding, L_{jk} = mutual inductance between j^{th} and k^{th} winding ($j \neq k$), and $j, k \in \{1, 2, 3, 4\}$.

The voltages v_1, v_2, v_3, v_4 are proportional to each other [16]. Hence we have $v_2 = nv_1$, $v_3 = v_1$ and $v_4 = nv_1$. For zero-ripple in i_1 and i_2, their time derivatives must be zero at all times. This provides the following analytical conditions for the inductances defined in (1):

$$nL_{14} = L_{24}, L_{23} = L_{34}, L_{24} = L_{44}, L_{13} = L_{33}, L_{14} = L_{34}, nL_{13} = L_{23} \tag{3.2}$$

Although achieving these conditions in the inductances is the end goal, these equations provide very little insight into the magnetic design process. What we need is a core structure and a method to do an approximate design which gives us the winding turns and conductor dimensions for each winding. This is explained in the next section. This reduces the problem to simply a matter of picking the correct air-gap at which the relationships in (2) will hold true, which is determined by Finite-Element-Modelling (FEM).

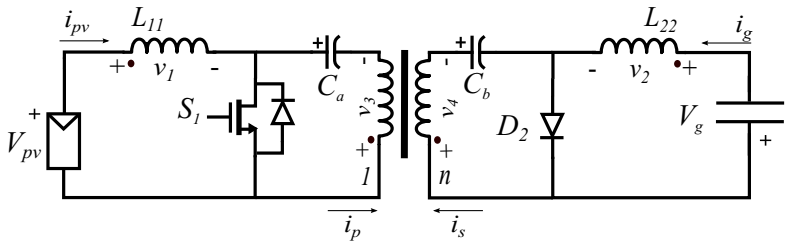

Figure 3.3: Uncoupled Isolated Ćuk converter

3.3 Area-Product of the Integrated Magnetic Core

In terms of the design method, the area-product approach[49, 50] is chosen over the geometrical constant methods (K_g and K_{gfe}) [49, 29] due to the ready availability of area-product data by vendors. The Area-Product Method is modified from its classical inductor design counterpart to design this four-winding coupled inductor structure to suit the application and incorporate the zero current ripple condition. The formulation of the area-product requires consideration of the following:

3.3.1 Magnetizing Inductance of the Isolation Transformer

The basic idea for zero-ripple is to shift the current ripple in windings 1 & 2 (input and output inductors) to the magnetizing inductance of the isolation transfomer (Windings 3 & 4) via a coupled magnetic pathway as explained by Ćuk in [51]. For this purpose, initially we consider that the input and output inductors are kept separate from the isolation transformer (in an isolated Ćuk converter) in Fig. 3.3, and we designed the input and output inductors according to their ripple specification (same for both), for the peak-to-peak ripple in each, we would have:

$$\Delta i_{L_{11}} = f_r I_{pv} \tag{3.3}$$

$$\Delta i_{L_{22}} = f_r I_g \tag{3.4}$$

where f_r = fraction of dc value of the corresponding inductor currents, and I_{pv} and I_g are the dc values of the currents through windings 1 and 2 respectively. If the peak-to-peak ripple in magnetizing current is Δi_M, then we have total ripple in the magnetizing inductance (referred to primary) as

$$\Delta i_M = \Delta i_{M|\text{transformer}} + \Delta i_{M|\text{inductors}}$$
$$\approx \Delta i_{M|\text{inductors}} = \Delta i_{L_{11}} + n\Delta i_{L_{22}} = f_r(I_{pv} + nI_g) \quad (3.5)$$

since the ripple due to just the transformer magnetizing current is approximately zero because the windings 3 and 4 are tightly coupled.

For a fully-efficient Ćuk converter,

$$I_g = \frac{I_{pv}(1-D)}{nD} \quad \text{where} \quad D \quad = \text{duty-ratio of } S_1 \quad (3.6)$$

During the interval when S_1 is on, a voltage of V_{pv} is applied across the magnetizing inductance, since the steady state voltage across C_a (Fig. 3.2) is V_{pv}. This gives:

$$\Delta i_M = \frac{V_{pv}D}{L_p f_s} \quad (3.7)$$

where f_s = switching frequency, L_p = isolation transformer magnetizing inductance. From (5)-(6) we have

$$\Delta i_M = \frac{f_r I_{pv}}{D} \quad (3.8)$$

From (7) and (8), then

$$L_p = \frac{D^2 Z_{pv}}{f_r f_s} \quad (Z_{pv} = \text{PV source impedance}) \quad (3.9)$$

Since the converter will operate at the maximum power point of the PV panel for maximum utilization, it seems reasonable to pick

$$L_p = \frac{D_{max}^2 Z_{MPP}}{f_r f_s} \quad (3.10)$$

where $Z_{MPP} = Z_{pv}$ at maximum power point. For a PV panel, the stable region of operation is to the right of the maximum power point (MPP) on the P-V curve. For any given battery voltage, operation at maximum duty ratio of a Ćuk converter corresponds to the MPP (hence $D_{MPP} = D_{max}$).

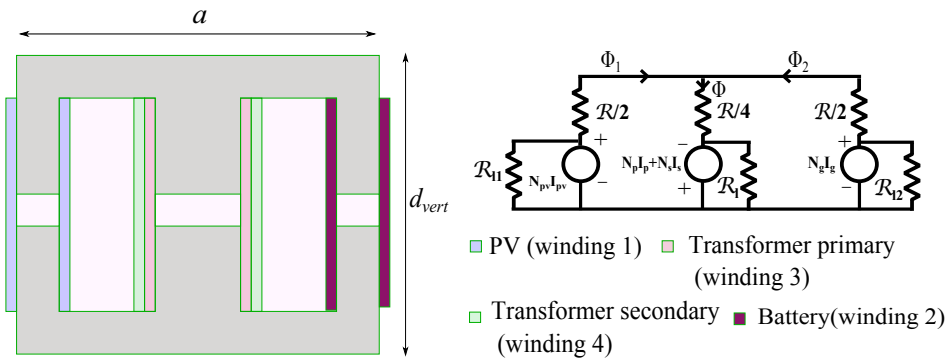

Figure 3.4: Core Structure and Flux Reluctance Model

3.3.2 Core Structure, Zero-ripple and Peak Flux Density

An EE-core with the same air gap across all the limbs is chosen for symmetry reasons and tunability as explained in [45]. The windings are placed as shown in Fig. 3.4. The difference from the conventional transformer lies in the fact the windings on the center limb have an air-gap as opposed to a conventional transformer, apart from being coupled to two other inductors. The reason for this is because it allows better control of the reluctance of the core and makes it less sensitive to error [52]. At very low air-gap, the inductances vary rapidly and the design point is not suited for the zero-ripple phenomenon. However, although the air-gap increases leakage between windings 1 and 3, 2 and 4, the windings 3 and 4 are still tightly coupled and the voltages in them proportional. The corresponding flux-reluctance circuit is obtained by removing several negligible leakage flux components and clubbing together the others similar to [46]. The reluctances are defined in terms of a reluctance parameter $\mathcal{R}$, where

$$\mathcal{R} = \frac{2x}{\mu_0 A_c} \quad (\frac{x}{2} = \text{spacer airgap}) \tag{3.11}$$

$\mathcal{R}/2$ and $\mathcal{R}/4$ represent the reluctances due to air-gap in the three limbs, while $\mathcal{R}_l$, $\mathcal{R}_{l1}$ and $\mathcal{R}_{l2}$ represent those due to leakage as shown in Fig. 3.4. The zero-ripple condition derived in [53] dictates that:

$$\frac{N_{pv}}{N_p} = 2 + \frac{x}{l} = f \tag{3.12}$$

where l = "leakage parameter"[45]. The leakage parameter has the dimensions of length and models the center limb leakage flux path, i.e., $\mathcal{R}_l = \frac{l}{\mu_0 A_c}$. '$f$' is a turns ratio

which is later used in deriving the area product.
N_{pv} = No. of turns of winding 1, N_p = No. of primary turns (winding 3).

$$N_s(\text{secondary turns(winding 4)}) = nNp \tag{3.13}$$

$$N_g(\text{winding 2}) = nN_{pv} \tag{3.14}$$

Applying KCL and KVL to the magnetic circuit of Fig. 3.4 yields:

$$N_{pv}i_{pv} + \phi_1\frac{\mathcal{R}}{2} + \phi\frac{\mathcal{R}}{4} + N_p i_p + N_s i_s = 0 \tag{3.15}$$

$$N_g i_g + \phi_2\frac{\mathcal{R}}{2} + \phi\frac{\mathcal{R}}{4} + N_p i_p + N_s i_s = 0 \tag{3.16}$$

$$\phi = \phi_1 + \phi_2 \tag{3.17}$$

Solving (15)-(17) for ϕ_1, ϕ_2 and ϕ yields the following equations:

$$\phi_1 = \frac{1.5N_{pv}i_{pv} - 0.5N_g i_g + N_p i_p + N_s i_s}{\mathcal{R}} \tag{3.18}$$

$$\phi_2 = \frac{1.5N_g i_g - 0.5N_{pv}i_{pv} + N_p i_p + N_s i_s}{\mathcal{R}} \tag{3.19}$$

$$\phi = \frac{N_{pv}i_{pv} + N_g i_g + 2(N_p i_p + N_s i_s)}{\mathcal{R}} \tag{3.20}$$

Peak flux densities are needed to in order to find the correct core cross-sectional area A_c. To find it, we use the following assumptions:

- i_{pv} and i_g are purely dc. (Zero-ripple terminal currents)
- The converter is 100% efficient: $\frac{V_g I_g}{V_{pv} I_{pv}} = 1$.
- $\frac{V_g}{V_{pv}} = \frac{nD}{1-D}$. This equation ceases to be valid beyond $D > 0.75$ due to the influence of parasitic resistances.

Using the above two assumptions, and the first equation in (6), we can show that (Refer Appendix A) at quasi-steady state the peak flux densities corresponding to ϕ_2, ϕ_1, ϕ

are

$$\hat{B_2} = \frac{N_{pv} I_{pv} f_{\phi_2}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R} A_c} \tag{3.21}$$

$$\hat{B_1} = \frac{N_{pv} I_{pv} f_{\phi_1}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R} A_c} \tag{3.22}$$

$$\hat{B} = \frac{N_{pv} I_{pv} f_{\phi}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R} A_c} \tag{3.23}$$

where

$$f_{\phi_2}(D) = \frac{2(1.5 - 2D)}{D} \tag{3.24}$$

$$f_{\phi_1}(D) = 2\left(2 - \frac{0.5}{D}\right) \tag{3.25}$$

$$f_{\phi}(D) = \frac{1}{D} \tag{3.26}$$

The second term in the above three expressions (24)-(26) is common for all the three limbs. Assuming that the converter operates close to the MPP of the PV panel, the quantity $N_{pv} I_{pv}$ is fairly constant. Therefore, f_{ϕ_2}, f_{ϕ_1} and f_{ϕ} decide the peak flux densities in the core. These functions are plotted in Fig. 3.5. It is seen that the limb with winding 1 has the most flux density for $D <= 0.5$ while the limb with winding 2 has the most flux density for $D >= 0.5$. The absolute maximum flux density across the three limbs of the core is $B_{peak} = \hat{B}_{\phi_2}|_{D=0.3}$ for $D \in (0.3, 0.75)$. Another interesting observation is that the peak flux density increases rapidly beyond $D = 0.3$. We see why it is a good choice to limit the minimum value of D to 0.3.

3.3.3 Window Area

The primary, secondary and the PV windings (windings 1,3 and 4) are in the left window of the EE-core while the primary, secondary and the battery windings (windings 2,3 and 4) as shown in Fig. 3.6. Using equations (6) and (12)-(14), the window areas can be expressed as (k_{Cu} is the fill factor and J_{rms} is the current density in all the windings)

$$A_{w1} = \frac{f N_p I_{pv} + N_p i_{p,rms} + n N_p i_{s,rms}}{k_{Cu} J_{rms}} = \frac{a_{w1} f N_p I_{pv} + N_p i_{p,rms} + n N_p i_{s,rms}}{k_{Cu} J_{rms}} \tag{3.27}$$

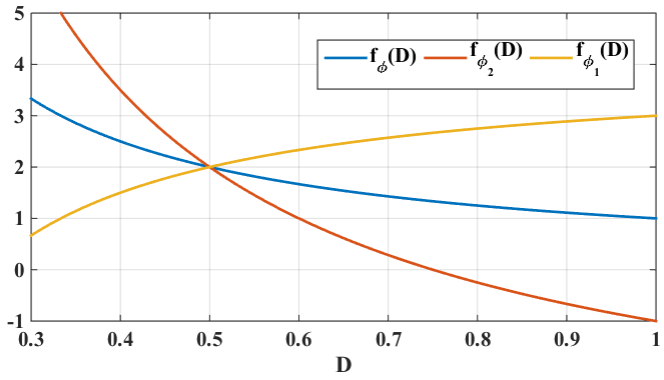

Figure 3.5: Determination of max. flux density

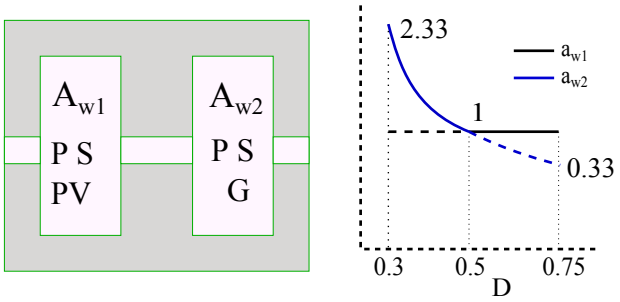

Figure 3.6: Window Area Determination

if the left window is used to design the core, and

$$A_{w2} = \frac{\frac{1-D}{D} f N_p I_{pv} + N_p i_{p,rms} + n N_p i_{s,rms}}{k_{Cu} J_{rms}} = \frac{a_{w2} f N_p I_{pv} + N_p i_{p,rms} + n N_p i_{s,rms}}{k_{Cu} J_{rms}} \tag{3.28}$$

if the right window is used to design the core.

where $a_{w1} = 1$ and $a_{w2} = \frac{1-D}{D}$. It is evident that a_{w1} and a_{w2} decide which window area is larger and at what duty ratio. These are plotted in Fig. 3.6 as a function of D. It is seen that selecting a_{w2} (henceforth A_{w2}) at $D = 0.3$ takes care of the entire design space, since in the actual physical core, both window areas are identical, and this will

be the worst case design. The final expression is:

$$max(A_w) = A_{w2}|_{D=0.3} = \left(\frac{N_g I_g + N_p I_p + N_s I_s}{k_{Cu} J_{rms}} \right) \Bigg|_{D=0.3} \tag{3.29}$$

It is seen that the worst cases occur at $D = 0.3$ for both peak flux density and window area. Hence it would be a natural choice to define the worst case area product at this point, as will be demonstrated in the next section.

3.3.4 Area Product

$D \in (0.3, 0.5)$:

From (13) & (22) (peak flux density),

$$N_p = \frac{\hat{B_1} A_c \mathcal{R}}{\frac{2f(1.5-2D)}{D} I_{pv} + 2 * max(i_p + n i_s)} \tag{3.30}$$

From (25) (window area),

$$N_p = \frac{A_{w2} k_{Cu} J_{rms}}{\frac{f(1-D)}{D} I_{pv} + i_{p,rms} + n i_{s,rms}} \tag{3.31}$$

$D \in (0.5, 0.75)$:

From (21) (peak flux density),

$$N_p = \frac{\hat{B_2} A_c \mathcal{R}}{2f I_{pv}(2 - \frac{0.5}{D}) + 2 * max(i_p + n i_s)} \tag{3.32}$$

From (25) (window area),

$$N_p = \frac{A_{w1} k_{Cu} J_{rms}}{f I_{pv} + i_{p,rms} + n i_{s,rms}} \tag{3.33}$$

The total core reluctance at sufficiently large air-gap seen by the windings 3 & 4 can be evaluated to $\mathcal{R}/2$. This is true when $\frac{x}{2} > \frac{10 l_m}{\mu_r}$, where l_m is the mean magnetic path length of the EE core and μ_r is the relative permeability of the Ferrite Core. This condition is derived in Appendix (B). Hence the primary magnetizing inductance is

$$L_p = \frac{2N_p^2}{\mathcal{R}} \tag{3.34}$$

From (30)-(34), we can deduce the area product:

$$A_p(\text{Area Product}) = A_c A_w = \frac{L_p I \hat{I}}{2\hat{B} k_{Cu} J_{rms}} \tag{3.35}$$

where $\hat{B} = \hat{B}_1$ if $D \in (0.3,0.5)$ and $\hat{B} = \hat{B}_2$ if $D \in (0.5,0.75)$. Also

$$\hat{I} = \begin{cases} 2fI_{pv}(\frac{1.5-2D}{D}) + 2 * max(i_p + ni_s) & \text{if } D \in (0.3, 0.5) \\ 2fI_{pv}(2 - \frac{0.5}{D}) + 2 * max(i_p + ni_s) & \text{if } D \in (0.5, 0.75). \end{cases} \tag{3.36}$$

and

$$I = \begin{cases} nfI_g + i_{p,rms} + i_{s,rms} & \text{if } D \in (0.3, 0.5) \\ fI_{pv} + i_{p,rms} + i_{s,rms} & \text{if } D \in (0.5, 0.75). \end{cases} \tag{3.37}$$

The expressions for $i_{p,rms}$ and $i_{s,rms}$ are derived in the Appendix(C). It can be seen that A_p is a complex function of D, provided the parameters of the PV panel are provided.

An iterative design algorithm is outlined in the flowchart of Fig. 3.7. Once an appropriate core is picked for the worst case design and N_p calculated, the air-gap is computed using an accurate expression of inductance (see Appendix(C)). This is necessary because the inductance varies very rapidly near zero air-gap and the approximate equation (31) is no longer adequate. However, we cannot use the actual equation in formulating the expression of area product because it requires knowledge of the mean magnetic length and core permeability, but the core is not yet known to us. The validity of the design is therefore verified by the condition $g = \frac{x}{2} < \frac{10 l_m}{\mu_r}$. If this condition is satisfied, it means the approximate equation (34) is valid and hence so is the area product expression. Additionally, the ratio N_{pv}/N_p needs to be fairly accurate, i.e., 2.25, hence the minimum integer value for N_p needs to be 4 in order to have integer number of turns on all the four windings. If either of these two conditions are violated, N_p needs to be increased from the intial value N_{p0}. However, now there is the additional problem that the windings will no longer fit in the core window according to (24)-(25). Hence a custom version of the original core with the same area product, but with a more skewed aspect ratio is needed as shown in the flowchart of Fig. 3.7.

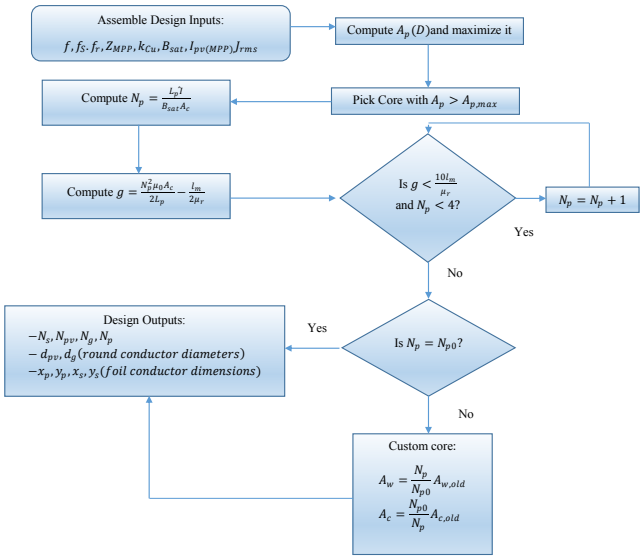

Figure 3.7: Core Selection and Winding Design Flowchart

3.4 Converter Specifications and Design Process

The specifications for the SW 270 mono panel [26] and other relevant design parameters chosen are outlined in Table I.

The material used is the 3C94 power ferrite available from Ferroxcube. The Ferrite is designed for use up to 300 kHz, beyond which core losses become significant. Please note that although B_{sat} for 3C94 material is specified as 0.47 T in the datasheet, a derating factor of approximately 70%[27] is applied to take into account thermal degradation, which means the actual value of B_{sat} used in the design is 0.33 T. The choice of factor f was due to guidelines given in [16]. With these constants, the area-product is plotted as a function of duty-ratio ($D' = 1 - D$) in Fig. 3.7.

In Fig. 3.8, A_{p1} denotes the expression of area product from (32) for $D \in (0.3,0.5)$ used for the entire $D \in (0.3,0.75)$ while A_{p2} denotes the expression of area product from (32) for $D \in (0.5,0.75)$ used for the entire $D \in (0.3,0.75)$. The worst case design for a particular duty ratio is highlighted in black for $D \in (0.3,0.75)$. Clearly, the worst case for the entire span is $D = 0.3$, which confirms our previous hypotheses in sections (III)B & (III)C. For the remainder of this section, subscripts 'pv','g','p' and 's' refer to windings 1,2,3 and 4 respectively.

Table 3.1: Specifications

Parameter	Value
f_r	0.6
Z_{MPP}	3.5 Ω
f_S	100 kHz
I_{pv}	9.44 A
J_{rms}	4 A/mm^2
k_{Cu}	0.4
μ_r	1790
f	2.25
B_{sat}	0.33 T

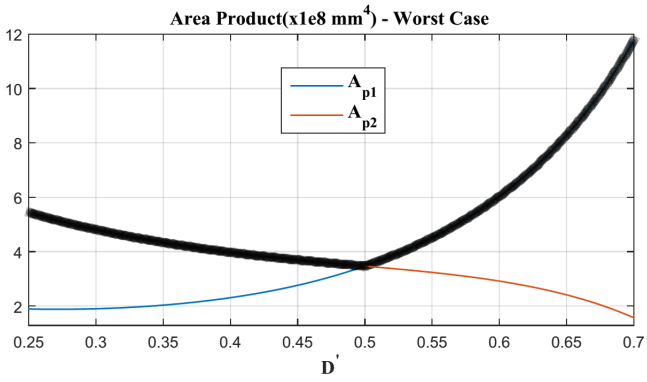

Figure 3.8: Area Product

For windings 1 & 2, since they have very low ripple, skin effect is considered negligible and so round conductors are used. The winding sizes were calculated using the following equations:

$$d_{pv} = \sqrt{\frac{4I_{pv}}{\pi J_{rms}}} \quad ; \quad d_g = \sqrt{\frac{4I_g}{\pi J_{rms}}} \tag{3.38}$$

Foil conductors are used for windings 3 & 4. The skin depth for Copper at 100 kHz is $\delta = 0.2$mm and the layer porosity factor is chosen to be $\eta_s = 0.9$. Then the maximum

number of turns per layer are:

$$nl_{p,max} = \left\lfloor \eta_s \sqrt{\frac{4}{\pi}} \frac{l_w}{d_p} \right\rfloor \quad \left(d_p = \sqrt{\frac{4i_{p,rms}}{\pi J_{rms}}} \right) \tag{3.39}$$

$$nl_{s,max} = \left\lfloor \eta_s \sqrt{\frac{4}{\pi}} \frac{l_w}{d_s} \right\rfloor \quad \left(d_p = \sqrt{\frac{4i_{s,rms}}{\pi J_{rms}}} \right) \tag{3.40}$$

Here d_p and d_s are the diameters if primary and secondary windings were built with round conductors. l_w is the window height of the selected core, with zero air-gap. These values are used for primary and secondary turns if $d_p, d_s < \delta$. Otherwise, turns per layer are given by:

$$nl_p = \frac{\eta_s l_w}{\left\lfloor \frac{\pi {d_p}^2}{4\delta} \right\rfloor} \quad ; \quad nl_s = \frac{\eta_s l_w}{\left\lfloor \frac{\pi {d_s}^2}{4\delta} \right\rfloor} \tag{3.41}$$

Foil widths:

$$y_p = \frac{\eta_s l_w}{\lfloor nl_p \rfloor} \quad ; \quad y_s = \frac{\eta_s l_w}{\lfloor nl_s \rfloor} \tag{3.42}$$

Foil thicknesses:

$$x_p = \frac{\pi {d_p}^2}{4y_p} \quad ; \quad x_s = \frac{\pi {d_s}^2}{4y_s} \tag{3.43}$$

Four primary and four secondary layers are interleaved to reduce proximity losses. For the given solar panel, the design outputs were obtained with a first pass of the algorithm. The outputs are given in Table II. The air-gap obtained using the flowchart (when the zero-ripple condition occurs in the input and output currents) is $g = 0.63$mm.

The core chosen was the standard Ferroxcube E65/32/27.

Finite Element Modelling : The core and wire sizes obtained as a result of the design procedure only give us a starting point in the design. The air-gap is now tuned using Finite-Element-Modelling methods for the zero-ripple condition. A flux density plot as a result of magnetostatic 2-D FEA (Finite-Element Analysis) on the selected core using ANSYS Maxwell is shown in Fig. 3.9. It can be seen that there is a tendency for the flux lines to crowd near the inner edges of the core. The extracted mutual inductances (L_{13} vs L_{33}), (L_{24} vs L_{44}) as a result of parametric sweeps of the air-gap are shown in Fig. 10. The plots of other relevant mutual inductances in equation (2), such as (L_{23} vs L_{34}) coincide and are not shown here.

The 2D FEA is approximate in the sense that the current return paths are infinite

Table 3.2: Design Outputs

Parameter	Value
N_p	10
N_s	50
N_{pv}	22
N_g	110
x_p	0.15 mm
x_s	0.208 mm
y_p	20 mm
y_s	3.1 mm
d_g	0.9 mm
d_{pv}	2 mm

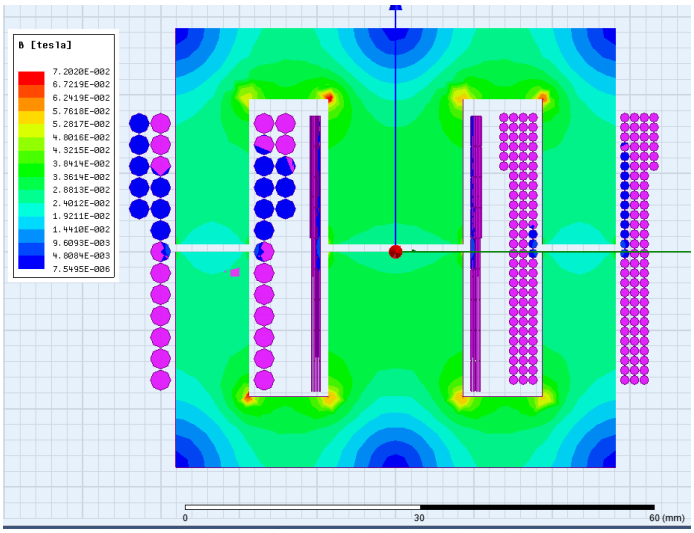

Figure 3.9: 2D core structure showing flux densities

and the inductance values are extracted per metre in the z-direction and then multiplied with z-dimension of the core. However, the computational time is an order of magnitude less than its 3D counterpart. According to this analysis, the optimum air-gap is approximately 1.8mm from Fig. 3.10, where equation (2) holds true.

The 3D FEA is performed using symmetry cuts to reduce computation time. The

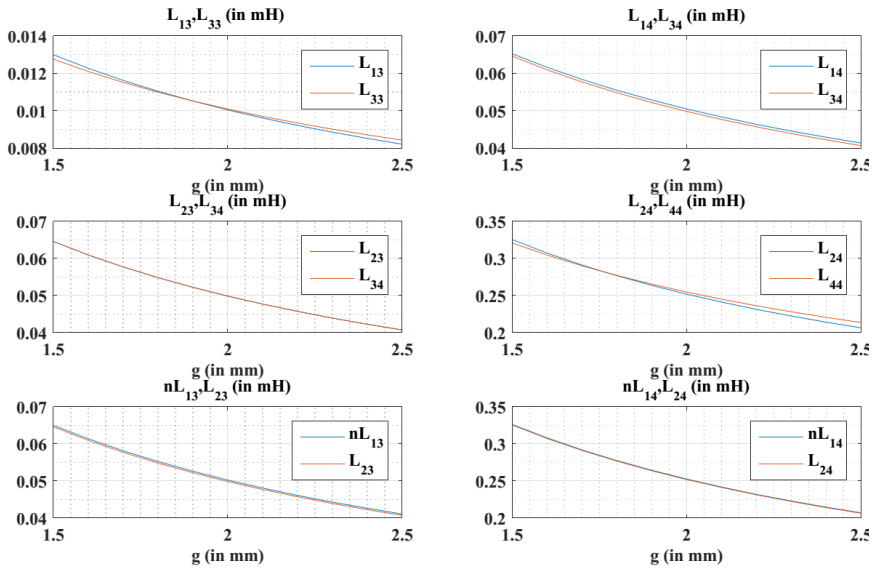

Figure 3.10: plots of the relevant quantities in (2) with 2D FEA

extracted mutual inductances (L_{13} vs L_{33})) as a result of parametric sweeps of the air-gap are shown in Fig. 3.11. The plots of other relevant mutual inductances in equation (2), such as (L_{23} vs L_{34}) coincide and are not shown here. The optimum air-gap in this case is 0.9mm. The air-gap calculated according to the formula $g = \frac{N_p^2 \mu_0 A_c}{2L_p} - \frac{l_m}{2\mu_r}$ from the flowchart in Fig. 7 is 0.63 mm and this is a bit different to the value obtained by FEM. The coupling coefficients extracted are as shown in Table III.

where k_{xy} = coupling coefficient between x^{th} winding and y^{th} winding. The self-inductances at this air-gap are: $L_{11} = 48.82$ μH, $L_{22} = 1.23$mH, $L_{33} = 12.68$ μH, $L_{44} =$

Table 3.3: Coupling Coefficients

Parameter	Value
k_{14}	0.50957
k_{12}	0.34138
k_{34}	0.99705
k_{23}	0.51044
k_{13}	0.50738
k_{24}	0.51247

319 μH.

The leakage parameter l for the completed design is calculated by rewriting (12).

$$l = \frac{x}{f-2} = 7.2 \text{ mm (since } \frac{x}{2} = 0.9 \text{ mm)}$$

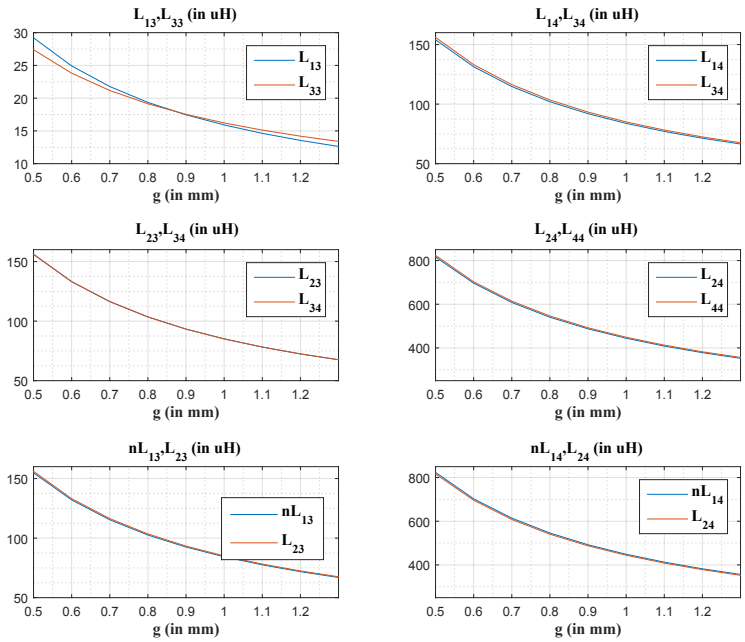

Figure 3.11: plots of the relevant quantities in (2) with 3D FEA

Thermal Validation: The ac part of the peak flux density from (21)-(23) in the core using (5)-(6) is given by

$$\hat{B}_{ac} = \frac{2 * max(N_p i_p + N_s i_s)}{\mathcal{R} A_c} = \frac{N_p \Delta i_M}{\mathcal{R} A_c} = \frac{N_p f_r I_{pv}}{D \mathcal{R} A_c} \tag{3.44}$$

$\hat{B}_{ac,max} = \hat{B}_{ac}|_{D=0.3} = 0.06$T while the total $\hat{B}_2|_{D=0.3} = B_{sat}$ =0.33T as shown in section III(B). The maximum core loss over the temperature range of 25-100^{0}C for this core material[28] at 100 kHz is 20 mW/cc. The E65/32/27 core has a volume of 79 mm^3. This means that the E65/32/27 core has a total maximum core loss of 1.58W. The ac winding resistances extracted by eddy current analysis in Ansys Maxwell at 100 kHz are given by: $R_{pv} = 6.91$ mΩ, $R_g = 0.1734$ Ω, $R_p = 7$ mΩ, $R_s = 0.1182$ Ω. At D=

0.3 and at rated power (250W), $I_{pv} = 9.44$ A, $I_g = 3.9$A, $i_{p,rms} = 12.34$A, $i_{s,rms} = 2.56$ A. The total copper loss is given by $P_{Cu} = I_{pv}^2 R_{pv} + I_g^2 R_g + i_{p,rms}^2 R_p + i_{s,rms}^2 R_s = 5.09$ W. Then the total magnetic loss is 6.67W. In accordance with [50], we have:

$$R_{\theta,rad} = \frac{T_{core} - T_{amb}}{0.0306a^2(0.01T_{core}^4 - 0.01T_{amb}^4)} \tag{3.45}$$

$$R_{\theta,conv} = \frac{1}{0.008a^2}\left(\frac{d_{vert}}{T_{core} - T_{amb}}\right)^{0.25} \tag{3.46}$$

$$R_{\theta,sa} = \frac{R_{\theta,rad}R_{\theta,conv}}{R_{\theta,rad} + R_{\theta,conv}} \tag{3.47}$$

where $R_{\theta,rad}$ is the radiative heat transfer thermal resistance, $R_{\theta,conv}$ is the convective heat transfer thermal resistance and $R_{\theta,sa}$ is the sink-to-ambient thermal resistance. T_{core} is the core temperature (uniform throughout[50]) while T_{amb} is the ambient temperature. The core dimensions a and d_{vert} are described in Fig. 3.4.

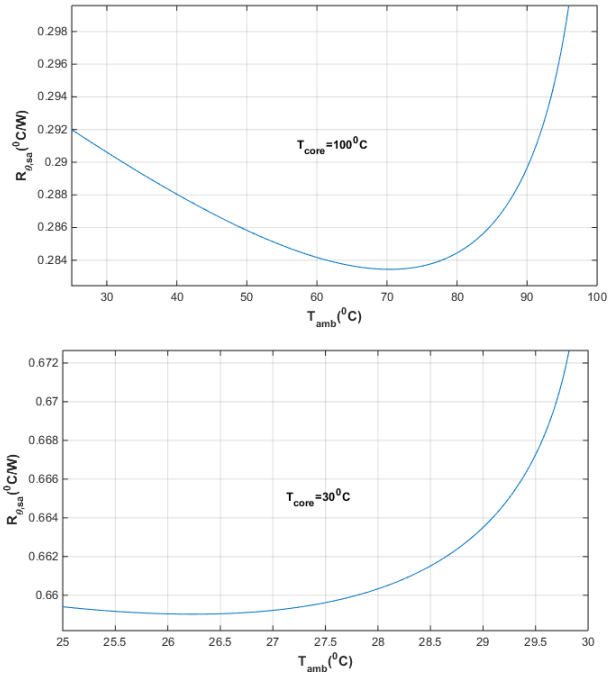

Figure 3.12: Sink-to-ambient Thermal Resistance ($R_{\theta,sa}$)

It is evident from Fig. 3.12 that $R_{\theta,sa}$ is more at lower core temperature than at higher core temperature. However, the value does not change by orders of magnitude

with change in core temperature. In fact, $R_{\theta,sa} \in (0.25, 0.7)$ for the temperature range under discussion. For a ballpark estimate, we choose $R_{\theta,sa}$=0.45^{0}C/W. Then the maximum body temperature rise above ambient of the core is then $\Delta T_{body,max}$= 0.45*6.67 = 3^{0}C which is insignificant.

Circuit Simulations: The integrated magnetic Ćuk converter is simulated in Cadence Pspice with the coupling coefficients extracted above. The FET (Field-Effect-Transistor) used is IRFB38N20D, while the diode is HFA50PA60C. Energy transfer capacitors C_a = 47 μF and C_b = 0.22 μF (Refer Fig. 1) are used for simulation.

The simulation results in PSpice using the coupling coefficients extracted by the FEA in Fig. 3.13 (under three different load conditions) show that the currents I_{pv} and I_g are low-ripple. The peak-to-peak ripple percentages are 2 and 3 respectively, which is much lesser than the standard ripple specification of 20% [54].

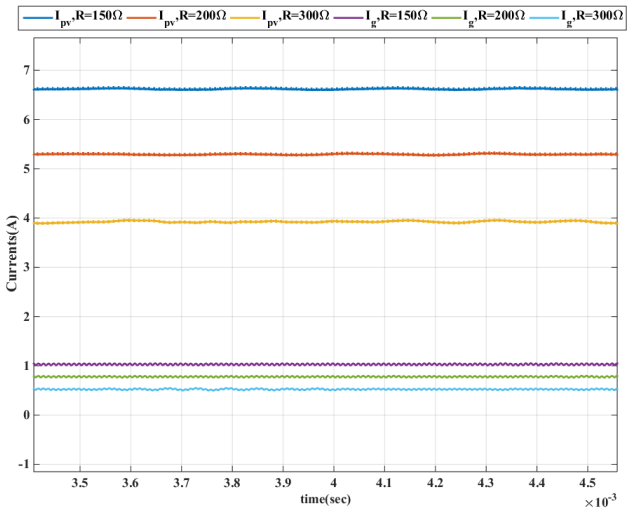

Figure 3.13: Simulated Terminal Currents under three different load conditions at D=0.5

Snubber Design and Efficiency: The leakage inductance of the isolation transformer can very well destroy the FET and diode. To keep the design simple, passive R-C damping is chosen. The snubberless design has a parasitic ringing frequency of 5 MHz. The FET and diode snubbers were chosen in accordance with the following equations:

$$R_{snub} = \sqrt{\frac{L_p}{C_p}}, \quad C_{snub} = \frac{1}{2\pi R_{snub}} \tag{3.48}$$

where L_p and C_p are the parasitic inductances and capacitances estimated at the switch nodes in accordance with [55]. The FET snubber was decided to be $R_{s1} = 0.22\ \Omega, C_{s1} = 5$ nF while the diode snubber was chosen to be $R_{s2} = 22\ \Omega, C_{s2} = 15$ nF. The efficiency vs load current I_g at $D = 0.5$, obtained from pspice simulations, is plotted in Fig. 3.14 (the winding resistances are obtained as a result of eddy current analysis in Maxwell is the ac resistance at 100 kHz). The peak efficiency is 95%.

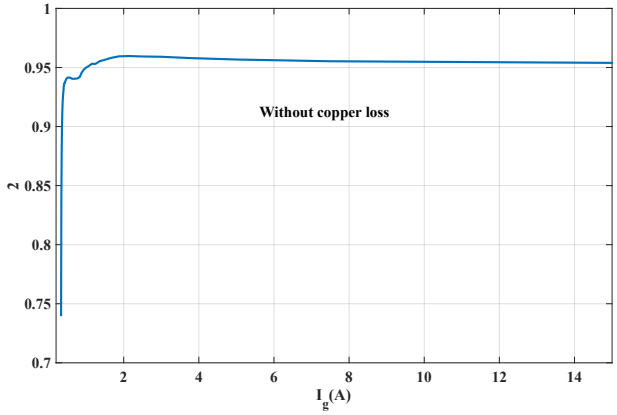

Figure 3.14: Efficiency plots

3.5 Experimental Results

The hardware setup for the integrated magnetic Ćuk converter is shown in Fig. 3.15. An adjustable structure with screw gauges on both sides is used for tuning the air-gap. The screw gauges have a pitch of 0.1mm. The switch used for S_1 in Fig. 3.2 is the MOSFET IRFB38N20D from Infineon, while the diode used for D_2 is HFA50PA60C from Vishay. The battery is emulated as a load resistor for demonstration purposes.

The Zynq 7000 FPGA along with the IRS 2110 gate driver was used to feed PWM signals into the Ćuk converter. For the PV side inductor winding, American Wire Gauge (AWG)#14 round magnet wire was used, while for the battery side winding AWG#20 round magnet wire was used. The transformer primary and secondary windings were wound with rectangular foil wire (.006" x.400" and .007" x .118" respectively). The self-inductances of the integrated core windings are measured by a network analyzer at a air-gap of 1.1mm and 100 kHz : $L_{11} = 47.5\ \mu$H, $L_{33} = 10\ \mu$H, $L_{44} = 310\ \mu$H, $L_{22} = 1.15$ mH. This delivers the closest match to the values obtained by 3-D FEM. The Ćuk

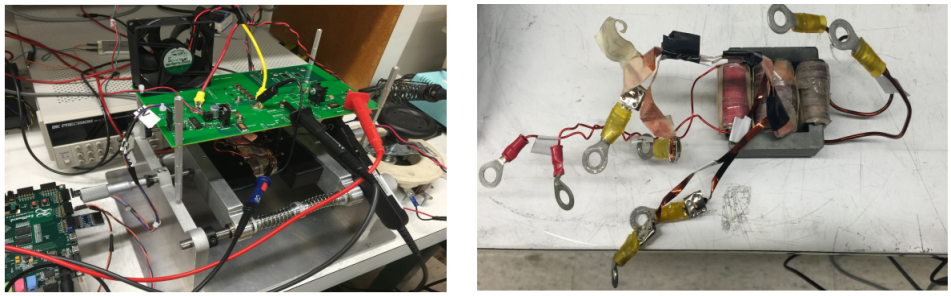

Figure 3.15: Hardware Setup and Integrated Magnetic Core

converter input/output waveforms for $D = 0.5$ are shown in Fig. 16-18 with respect to the drain-to-source voltages of the switch S_1. Figure 3.16 shows the performance at $V_{pv} = 15$ V and Output load resistance = 160 Ω where maximum efficiency is observed. The input power in this case is 70 W. The waveforms at full rated power (250 W) with $V_{pv} = 30$ V are shown in Fig. 3.17. The input and output current waveforms have very low fundamental ripple content. The input current has slightly higher ripple because of non-idealities in the practical development of the circuit, such as finite lead lengths of the magnetic windings. The output voltage is observed to be low ripple, as expected. The input and output current ac ripples for the currents in Fig. 3.17 are shown in Fig. 3.18. This is obtained by using the ac coupling option on the current probes. We see that the fundamental component of the ac ripple, i.e. at the switching frequency is close to zero as predicted. The higher order ripples are observed due to parasitic ringing and other converter non-idealities. As seen in Fig. 3.16, these ripples are not evident on the load current, but more on the input current. Δi_{pv} (pk-pk)= 0.6 A, or 6.67% of its peak dc value, which is 9 A. This is far above the recommended benchmark of 20% in [54] for inductor current ripples. The output voltage ripple is also less than 1%, while the recommended figure is 5% [54]. The experimental efficiency is 94% at full load, which very closely matches the simulation efficiency. A qualitative validation of the thermal analysis in the previous section was obtained by using an infra-red laser thermometer on the experimental setup which showed that there was no local hot-spot formation in and around the core.

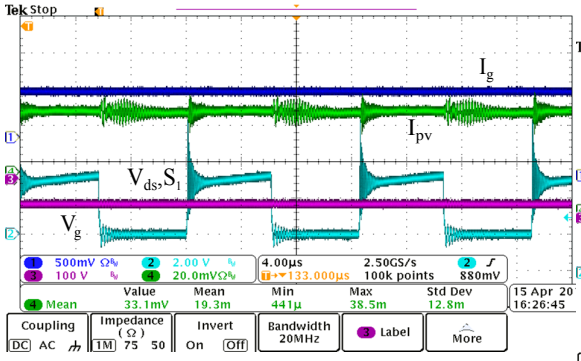

Figure 3.16: Input/Output signals at 25% rated power and half the rated V_{pv}(15V)

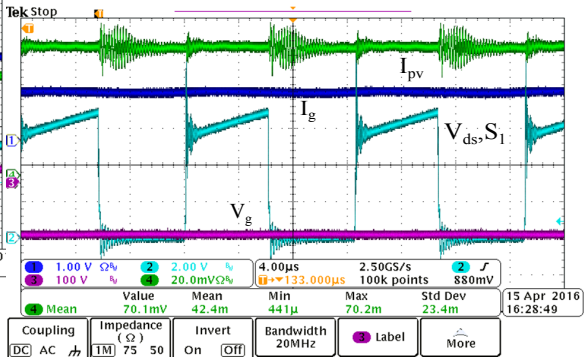

Figure 3.17: Input/Output signals at full rated power and full rated V_{pv}(30V)

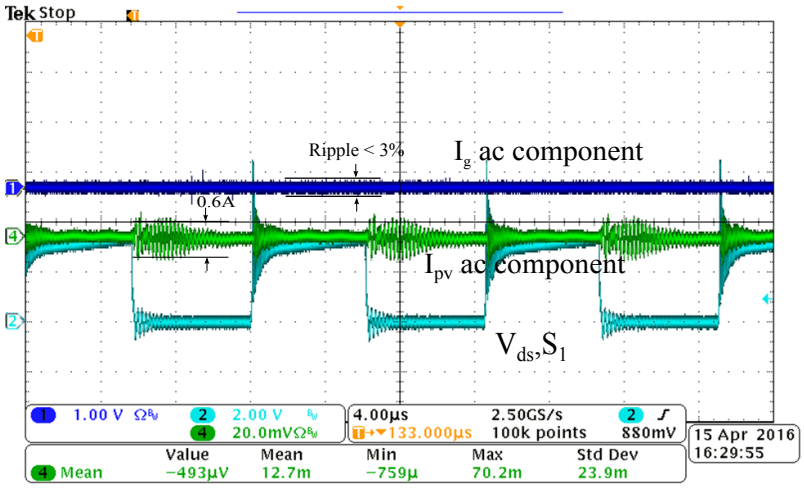

Figure 3.18: ac ripple on input and output currents

Chapter 4

Two-Port Integrated Magnetic Ćuk converter for PV-to-Grid Applications - Designed by Geometrical Constant (K_g) method

4.1 Introduction

DC-DC converters for interfacing PV panels to grid-tied inverters is a fairly common topic of discussion in contemporary power electronics. The boost converter tends to be the topology of choice [33, 34]. However,the problem of EMI (electromagnetic interference) in residential microgrids, as alluded to, in [33, 34] can be addressed better by the integrated magnetic Ćuk converter. The use of this converter is not novel in itself. An analytical condition on the inductance matrix can be derived which shows that the zero-ripple operation is theoretically possible, but the design of this magnetic structure is anything but straightforward. References [44, 45] discuss this, but are mostly semi-analytical and require several iterations, in addition to a priori estimate of winding leakages. Lack of a systematic method determining the power converter requirements into a viable magnetic design has prevented the Ćuk converter from being used.

This chapter places emphasis on the magnetic design process in the following way.

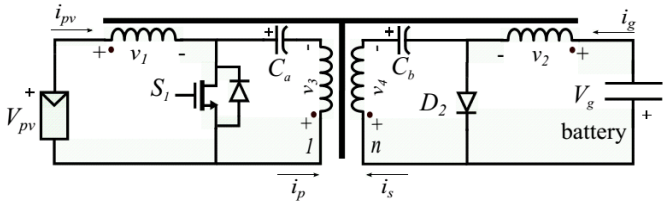

Figure 4.1: Complete System

Section II talks about the general requirements of a PV-to-grid DC-DC converter, and the inductance matrix requirements for zero-ripple. Section III describes the flux-reluctance model for the chosen magnetic structure and an approximate zero-ripple condition. The geometrical constant (K_g) is then derived using these approximate models in order to provide a systematic approximate design for this converter. The FEM (Finite Element Modelling) and simulation results are discussed that fine tune the design of this converter in Section IV. Section V presents conclusion and future work.

4.2 Description of the Converter

The converter schematic is shown in Fig. 4.1. The steady-state operable duty ratio is $D\in(0.3, 0.75)$. The upper limit is due to influence of non-idealities on the voltage conversion ratio, which is typically attributed to current-fed converters, such as the boost. The lower limit can be attributed to high peak flux density in the core, which is discussed later. The converter is designed to operate at a DC bus voltage of 340V at output with a solar panel which has same specifications as the SunModule Plus SW 270 mono (270 W) [56]. As such, this converter can be used for standalone residential applications among others.

For a four-winding coupled inductor, we have the following set of equations:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{12} & L_{22} & L_{23} & L_{24} \\ L_{13} & L_{23} & L_{33} & L_{34} \\ L_{14} & L_{24} & L_{34} & L_{44} \end{bmatrix} \times \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \tag{4.1}$$

The voltages v_1, v_2, v_3, v_4 are proportional to each other. For zero-ripple in i_1 and

i_2, their time derivatives must be zero at all times. This gives:

$$nL_{14} = L_{24}, L_{23} = L_{34}, L_{24} = L_{44}, L_{13} = L_{33}, L_{14} = L_{34}, nL_{13} = L_{23} \tag{4.2}$$

This says very little about the design process. What we need is a core structure and a method to do an approximate design which gives us the winding turns and conductor dimensions for each winding. This is explained in the next section. This reduces the problem to simply a matter of picking the correct air-gap at which the relationships in (2)-(3) will hold true, which is done by FEM.

4.3 Principle of Operation and Geometrical Constant

4.3.1 Magnetizing Inductance

The basic idea for zero-ripple is to shift the total interface winding ripple (windings 1 & 2) to the magnetizing inductance of the isolation transfomer (Windings 3 & 4 in Fig. 4.1) as explained by Ćuk in [51]. The other quantities are as labeled in Fig. 4.1. If the peak-to-peak ripple in magnetizing current is Δi_M, then let us impose the requirement

$$\Delta i_M = f_r(i_{1,rms} + n i_{2,rms}) \quad \text{where} \quad i_{1,rms} = I_{pv}; i_{2,rms} = I_g \tag{4.3}$$

since i_1 and i_2 are zero-ripple quantities. For a Ćuk converter (ideally),

$$I_g \approx \frac{I_{pv}(1-D)}{nD}; \Delta i_M = \frac{V_{pv} D}{L_p f_s} \tag{4.4}$$

where D = duty-ratio of S, f_s = switching frequency, L_p = isolation transformer magnetizing inductance. From (4) and (5) we have

$$\Delta i_M = \frac{f_r I_{pv}}{D} \tag{4.5}$$

From (4) and (5), then $L_p = \frac{D^2 Z_{pv}}{f_r f_s}$. Since the converter will most likely operate at the maximum power point of the PV panel for maximum efficiency, it seems reasonable to pick

$$L_p = \frac{D_{max}^2 Z_{MPP}}{f_r f_s} \tag{4.6}$$

where Z_{MPP} = PV source impedance at maximum power point. Now usually for

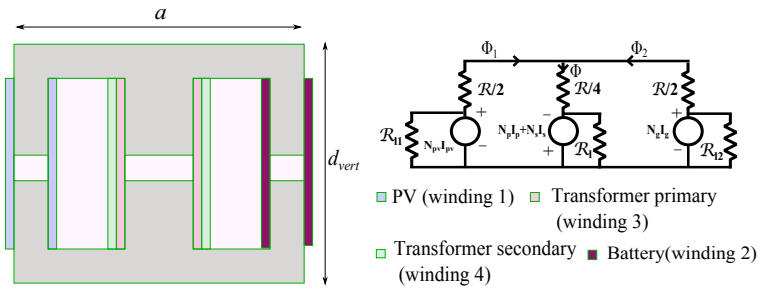

Figure 4.2: Core Structure and Flux Reluctance Model

a PV panel, the stable region is to the right of the MPP (maximum power point). If the grid voltage is asssumed to be constant throughout, then the maximum duty ratio of a Ćuk converter corresponds to the MPP. Also, from Fig. 4.2, the total reluctance seen by the primary winding which links the ferrite core is $\mathcal{R}/2$, assuming the air-gap is large enough. Hence we also have $L_p = \frac{2N_p^2}{\mathcal{R}}$.

4.3.2 Core Structure, Zero-ripple and Peak Flux Density

An EE-core with a spacer air gap is chosen for symmetry reasons and tunability as explained in [45, 46].The core structure and the corresponding intuitive flux-reluctance model is shown in Fig. 4.2. The reluctances are defined in terms of $\mathcal{R} = \frac{2x}{\mu_0 A_c}$ where $\frac{x}{2}$ = spacer airgap. $\mathcal{R}/2$ and $\mathcal{R}/4$ represent the reluctances due to air-gap, while $\mathcal{R}_l$, $\mathcal{R}_{l1}$ and $\mathcal{R}_{l2}$ represent those due to leakage. The zero-ripple condition is derived in [53]. It is given by:

$$\frac{N_{pv}}{N_p} = f = 2 + \frac{x}{l} \tag{4.7}$$

where l = leakage parameter[4], N_{pv} = No. of turns of winding 1, N_p = No. of primary turns (winding 3). Also N_s(secondary turns(winding 4)) = nNp, N_g(winding 2) = nN_{pv}. As shown in [9], at quasi steady-state the peak flux densities corresponding to ϕ_2, ϕ_1, ϕ are:

$$\hat{B}_2 = \frac{N_{pv}I_{pv}f_{\phi_2}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R}A_c} \quad \text{where} \quad f_{\phi_2}(D) = \frac{2(1.5 - 2D)}{D} \tag{4.8}$$

$$\hat{B}_1 = \frac{N_{pv}I_{pv}f_{\phi_1}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R}A_c} \quad \text{where} \quad f_{\phi_1}(D) = 2\left(2 - \frac{0.5}{D}\right) \tag{4.9}$$

$$\hat{B} = \frac{N_{pv}I_{pv}f_{\phi}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R}A_c} \quad \text{where} \quad f_{\phi}(D) = \frac{1}{D} \tag{4.10}$$

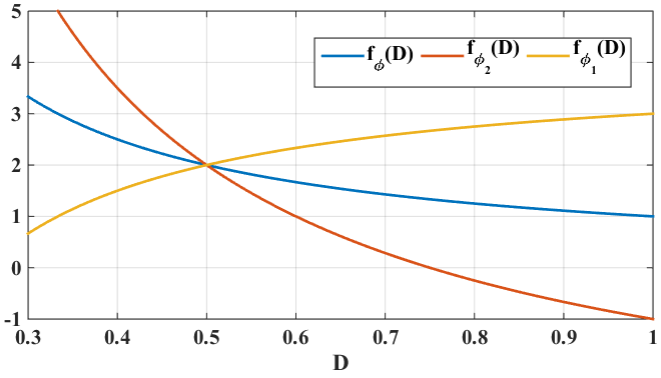

Figure 4.3: Determination of max. flux density

The second term in the above three expressions is common for all the three limbs. Assuming that the converter operates close to the MPP of the PV panel, the quantity $N_{pv}I_{pv}$ is fairly constant. Therefore, f_{ϕ_2}, f_{ϕ_1} and f_{ϕ} decide the peak flux densities in the core. These functions are plotted in Fig. 4. It is seen that the limb with winding 1 has the most flux density for $D <= 0.5$ while the limb with winding 2 has the most flux density for $D >= 0.5$. The absolute maximum flux density across the three limbs of the core is $B_{peak} = \hat{B}_{\phi_1}|_{D=0.3}$ for $D \in (0.3, 0.75)$. Another interesting observation is that the peak flux density increases rapidly beyond $D = 0.35$. We see why it is a good choice to limit the minimum value of D to 0.3.

4.3.3 Optimal Window Area Allocation

The fractions of the window area allotted to the windings are α_{pv} (winding 1), α_g (winding 2), α_p (winding 3), α_s (winding 4). Then the total copper loss is:

$$P_{Cu,tot} = \frac{\rho}{A_w k_{Cu}} \left(\frac{N_{pv}^2 I_{pv}^2 (MLT)_s}{\alpha_{pv}} + \frac{N_g^2 I_g^2 (MLT)_s}{\alpha_g} + \frac{N_p^2 I_p^2 (MLT)_c}{\alpha_p} + \frac{N_s^2 I_s^2 (MLT)_c}{\alpha_s} \right) \tag{4.11}$$

and the respective MLTs (Mean-Length-Per-Turns) are defined according to the dimensions in Fig. 4.4:

$$MLT_c = 2(a+e)+2(b+e), \quad MLT_s = 2(\frac{a}{2}+d)+2(b+d), \quad MLT = a+f+b+g \tag{4.12}$$

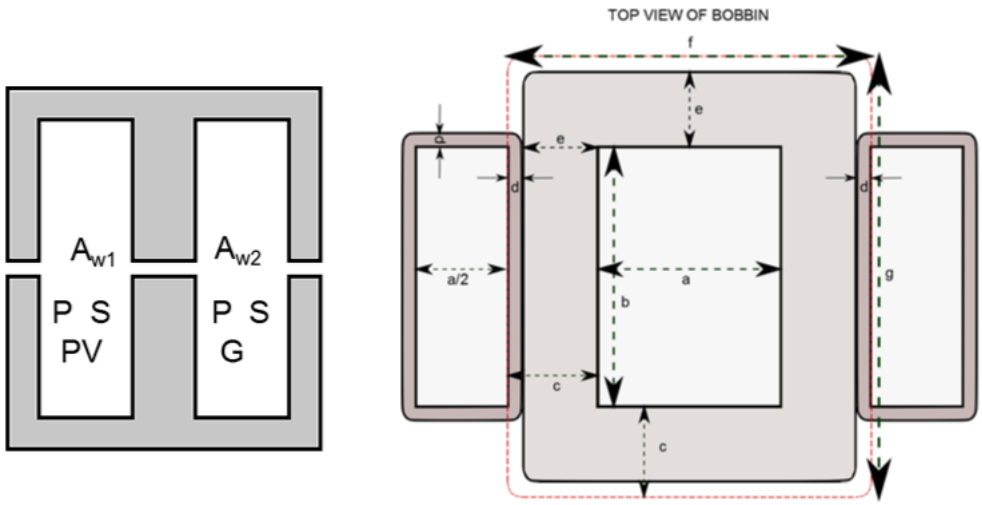

Figure 4.4: Optimal Window Area Allocation

where $d = e = \frac{f-a}{2}$ for the purpose of simplicity. ρ is the resistivity of copper. The quantity (MLT) is usually specified by bobbin manufacturers for standard transformer designs on the middle-limb of the EE core. We formulate a Lagrangian similar to [29, 49] to minimize copper loss.

$$f(\alpha_{pv}, \alpha_g, \alpha_p, \alpha_s) = P_{Cu,tot}(\alpha_{pv}, \alpha_g, \alpha_p, \alpha_s) + \xi_1 g_1(\alpha_{pv}, \alpha_g, \alpha_p, \alpha_s) + \xi_2 g_2(\alpha_{pv}, \alpha_g, \alpha_p, \alpha_s) \tag{4.13}$$

where ξ_1 and ξ_2 are the Lagrangian multipliers. The geometrical constraints are

$$g_1 = \alpha_{pv} + \alpha_p + \alpha_s - 1 = 0, \quad g_2 = \alpha_g + \alpha_p + \alpha_s - 1 = 0 \tag{4.14}$$

The optimal point (minimum copper loss) occurs where the following conditions are satisfied:

$$\frac{\partial f}{\partial \alpha_{pv}} = \frac{\partial f}{\partial \alpha_g} = \frac{\partial f}{\partial \alpha_p} = \frac{\partial f}{\partial \alpha_s} = 0 \tag{4.15}$$

Solving (15) gives

$$\alpha_{pv} = \alpha_g = \frac{\sqrt{m_s(N_{pv}^2 I_{pv}^2 + N_g^2 I_g^2)}}{D_{Cu}}, \quad \alpha_p = \frac{\sqrt{m_c} N_p i_{p,rms}}{D_{Cu}}, \quad \alpha_s = \frac{\sqrt{m_c} N_s i_{s,rms}}{D_{Cu}} \tag{4.16}$$

where

$$\begin{aligned} D_{Cu} &= \sqrt{m_s(N_{pv}^2 I_{pv}^2 + N_g^2 I_g^2)} + \sqrt{m_c}(N_p i_{p,rms} + N_s i_{s,rms}) \\ &= N_p(f\sqrt{m_s(I_{pv}^2 + n^2 I_g^2)} + \sqrt{m_c}(i_{p,rms} + n i_{s,rms})) \end{aligned} \tag{4.17}$$

Also $m_s = \frac{(MLT)_s}{MLT}$ and $m_c = \frac{(MLT)_c}{MLT}$ which denote ratios of MLTs. These ratios are chosen to be 0.5 in the formulation of the geometrical constant, which is the mean value of these quantities for a range of EE core sizes[12]. Substituting (16) in (11), the expression for optimal copper loss is

$$\begin{aligned} P_{Cu,opt} = \frac{\rho(MLT)D_{Cu}^2}{A_w k_{Cu}} \implies \frac{A_w}{MLT} &= \frac{\rho D_{Cu}^2}{k_{Cu} P_{Cu,opt}} \\ &= \frac{N_p^2(f I_{pv}\sqrt{m_s(\frac{2D^2-2D+1}{D^2})} + \sqrt{m_c}(i_{p,rms} + n i_{s,rms}))^2}{k_{Cu} P_{Cu,opt}} \end{aligned} \tag{4.18}$$

The expressions for $i_{p,rms}$ and $i_{s,rms}$ are derived in [48]. They are:

$$i_{p,rms} = \sqrt{T_1 + T_2 + T_3 + T_4} \quad \text{where} \quad T_1 = (1-D)I_{pv}^2, T_2 = D\left(0.5\Delta i_M - \frac{(1-D)I_{pv}}{D}\right)^2 \tag{4.19}$$

$$T_3 = \Delta i_M\left(0.5\Delta i_M - \frac{(1-D)I_{pv}}{D}\right)\frac{2D-D^2}{1-D}, T_4 = \Delta i_M^2 \frac{3D - D^2 + D^3}{3(1-D)^2} \tag{4.20}$$

$$i_{s,rms} = \sqrt{T_5 + T_6 + T_7 + T_8} \quad \text{where} \quad T_5 = \frac{(1-D)^2 I_{pv}^2}{Dn^2}, T_6 = (1-D)\left(\frac{I_{pv}}{n} + \frac{\Delta i_M}{2n}\right)^2 \tag{4.21}$$

$$T_7 = \Delta i_M\left(\frac{I_{pv}}{n} + \frac{\Delta i_M}{2n}\right)\frac{1-D^2}{nD}, T_8 = {\Delta i_M}^2 \frac{1-D^3}{3n^2 D^2} \tag{4.22}$$

4.4 Copper Loss Geometrical Constant

Using (7)-(11), and $L_p = \frac{2N_p^2}{R}$, we can obtain the following expression for the geometrical constant as

It can be shown analytically that I_{tot} and therefore K_g reaches its maximum at $D = 0.3$, which conforms to the worst-case duty ratio observation in section(B).

$D\in(0.3, 0.5)$: From (9), we have

$$N_p^2 = \left(\frac{\hat{B}_1 A_c \mathcal{R}}{\frac{2(1.5-2D)}{D} I_{pv} + 2 * max(i_p + ni_s)} \right)^2 \tag{4.23}$$

$D\in(0.5, 0.75)$: From (8), we have

$$N_p^2 = \left(\frac{\hat{B}_2 A_c \mathcal{R}}{2(2 - \frac{0.5}{D}) I_{pv} + 2 * max(i_p + ni_s)} \right)^2 \tag{4.24}$$

Finally, from (18) and (4) we have for $D\in(0.3, 0.75)$

$$N_p^2 = \frac{A_w k_{Cu} P_{Cu,opt}}{\rho(MLT)(f I_{pv} \sqrt{m_s(\frac{2D^2-2D+1}{D^2})} + \sqrt{m_c}(i_{p,rms} + ni_{s,rms}))^2} \tag{4.25}$$

Using (23)-(25) and $L_p = \frac{2N_p^2}{R}$, we can show

$$K_g(D) = \frac{A_c^2 A_w}{MLT} = \frac{\rho {L_p}^2 \hat{I}^2 I_{tot}^2}{4 k_{Cu} \hat{B}^2 P_{Cu,opt}} \quad \text{where} \tag{4.26}$$

$\hat{B} = \hat{B}_1$ if $D\in(0.3, 0.5)$ and $\hat{B} = \hat{B}_2$ if $D\in(0.5, 0.75)$. Also

$$I_{tot} = f I_{pv} \sqrt{m_s(\frac{2D^2 - 2D + 1}{D^2})} + \sqrt{m_c}(i_{p,rms} + ni_{s,rms}) \tag{4.27}$$

$$\hat{I} = \begin{cases} 2I_{pv}(\frac{1.5-2D}{D}) + 2 * max(i_p + ni_s) & \text{if } D\in(0.3, 0.5) \\ 2I_{pv}(2 - \frac{0.5}{D}) + 2 * max(i_p + ni_s) & \text{if } D\in(0.5, 0.75). \end{cases} \tag{4.28}$$

4.5 Converter Specifications and Design Process

The specifications for the SW 270 mono panel, and other relevant design parameters chosen were:

Table 4.1: Converter Specifications

f_r	Z_{MPP}	f_S	I_{pv}	$P_{Cu,opt}$	B_{sat}	k_{Cu}	μ_r	f	ρ(Copper)
0.6	3.5 Ω	100 kHz	9.44 A	2.5 W	0.2 T	0.4	1790	2.25	1.724e-6 Ω-cm

The copper loss is chosen to be 1% of the full power capacity, 250 W. The normalized version of $\frac{A_w}{MLT}$ is defined as $a_w = \frac{A_w k_{Cu} P_{Cu,opt}}{(MLT)N_p^2}$. It is plotted vs $D' = 1 - D$ in Fig. 4.5. The plot shows that the worst case happens at $D = 0.3$, similar to the peak flux density earlier. The plot of the geometrical constant is shown in Fig. 4.6. K_{g1} represents the geometrical constant if $\hat{I}_{D\in(0.3,0.5)}$ is used for the entire $D\in(0.3, 0.75)$ while, K_{g2} represents the geometrical constant if $\hat{I}_{D\in(0.5,0.75)}$ is used for the entire $D\in(0.3, 0.75)$. It is seen that the worst case happens at $D = 0.3$ for K_{g1}, which coincides with the previous plots of Window Area/Mean-Length-Per-Turn and Core Area.

An iterative design algorithm is outlined in the flowchart of Fig. 4.7. Once an appropriate core is picked for the worst case design and N_p calculated, the air-gap is computed using an accurate expression of inductance. This is necessary because the inductance varies very rapidly near zero air-gap and the approximate equation $L_p = \frac{2N_p^2}{\mathcal{R}}$ is no longer adequate. However, we cannot use the actual equation in formulating the expression of geometrical constant because it requires knowledge of the mean magnetic length and core permeability, but the core is not yet known to us. The validity of the design is therefore verified by the condition $g = \frac{x}{2} < \frac{10 l_m}{\mu_r}$. If this condition is satisfied, it means the approximate equation is valid and hence so is the area product expression. Additionally, the ratio N_{pv}/N_p needs to be fairly accurate, i.e., 2.25, hence the minimum integer value for N_p needs to be 4 in order to have integer number of turns on all the four windings. If either of these two conditions are violated, N_p needs to be increased from the intial value N_{p0}. However, now there is the additional problem that the windings will no longer fit in the core window according to (18). Hence a custom version of the original core with the same geometrical constant, but with a more skewed aspect ratio is needed as shown in the flowchart of Fig. 4.7.

The design outputs for the given set of converter specifications (Table I) using the flowchart are given in Table II. The core chosen was the standard Ferroxcube E55/28/25.

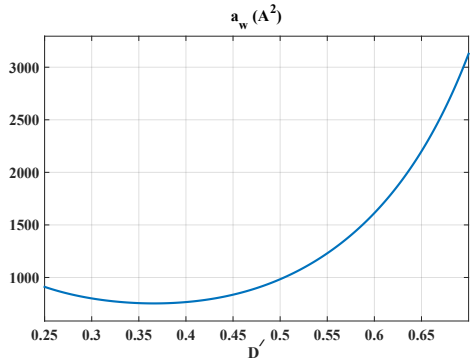

Figure 4.5: Window Area/ (Mean-Length-per-turn)

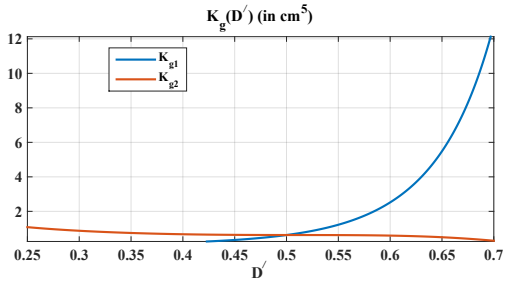

Figure 4.6: Copper Loss Geometrical Constant

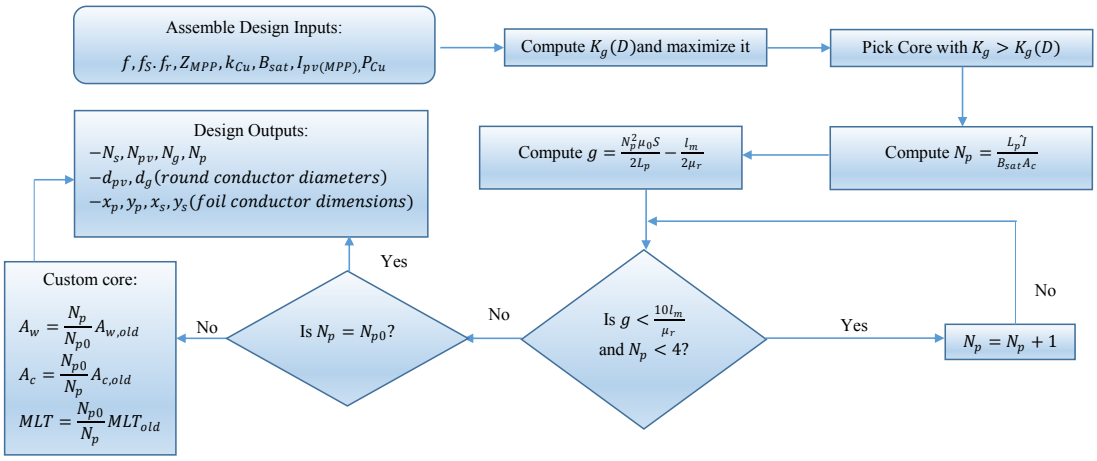

Figure 4.7: Core Selection and Winding Design Flowchart

Table 4.2: Design Outputs

N_p	N_s	N_{pv}	N_g	d_{pv}	d_g	x_p	x_s	y_p	y_s
6	30	13	65	2.6 mm	1.2 mm	0.185 mm	0.192 mm	16.7 mm	3.3 mm

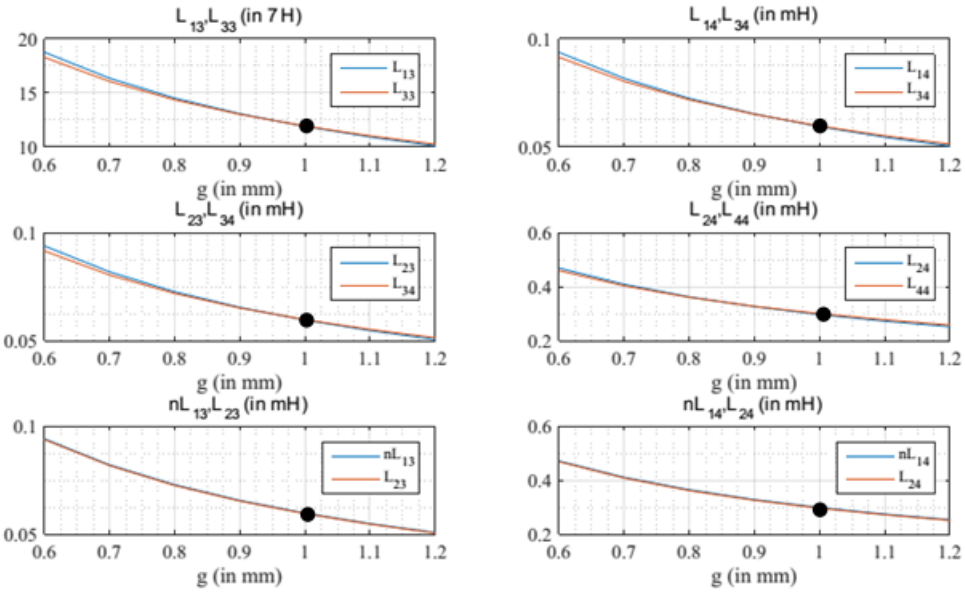

Figure 4.8: FEA Results

The wire sizes are chosen according to guidelines given in [48]. Round wires are chosen for windings 1 and 2 while foil conductors are chosen for windings 3 and 4. d_{pv} and d_g are diameters of windings 1 and 2, x_p and x_s are foil conductor thicknesses of windings 3 and 4, while y_p and y_s represent foil conductor heights. The results of FEA on this core using ANSYS Maxwell are shown in Fig. 4.8. These include plots of the inductances in (1) vs air-gap. The equations (2) are approximately satisfied at g=$\frac{x}{2}$=1.0mm, as shown by the black dots in Fig. 4.8. The coupling coefficients are extracted at this air-gap are used in a PSpice simulation. The peak-to-peak ripple percentages observed in I_{pv} and I_g are 1.61% and 3.75% as shown in Fig. 4.9(a). The slightly higher ripple in the output current is because the output inductor is not connected to perfect DC sources.

Efficiency: The converter is operated without snubber initially, and the peak efficiency is 94% around $R_{load} \approx 400\Omega$, although it demonstrates a fairly flat efficiency of 92% up unto that point (Fig. 4.9(b)). For a design with passive R-C snubbers (MOSFET snubber : $R_{s1} = 0.22\Omega, C_{s1} = 20nF$, diode snubber : $R_{s2} = 22\Omega, C_{s2} = 5nF$, the

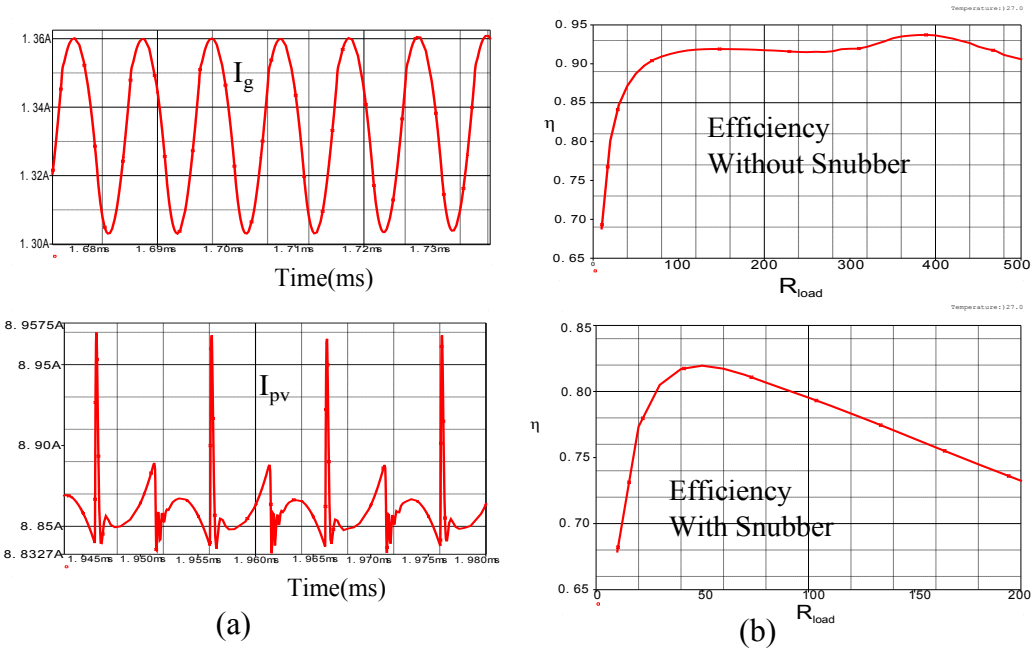

Figure 4.9: Simulation Results: Terminal currents

peak efficiency of 82% (Fig.6) occurs at $R_{load} \approx 50\Omega$. The snubbers are chosen according to the parasitic ringing frequency observed at the switch nodes, which is usually around 5 MHz.

Chapter 5

Soft-Switching Scheme in Three-port Converter with Integrated Magnetics

5.1 The Active-Clamp Soft-Switching Ćuk Converter

The Ćuk converter is optimal for PV conversion primarily because of its wide dynamic range. It is also able to effectively operate as a dc transformer because of clean input and output currents via means of integrated magnetics [59]. Other improvements on the basic Ćuk converter include the active-clamp technique proposed in [60]. This non-isolated Ćuk converter achieves ZVS turn-on of all the active switches. The isolated topology proposed in [61] also achieves ZVS turn-on but uses a second transformer and diode on the input side in addition to the additional components suggested in [60]. The method proposed in [62] for the isolated converter utlises the leakage inductance of the isolation transformer and the clamp capacitor to achieve resonance. However, the clamp capacitor is in principle supposed to be a fixed voltage source. Also, none of these topologies utilise the integrated magnetics extension of the Ćuk converter.

A two-port version of this converter was proposed in our earlier work [63]. This chapter builds extends the work to a three-port design. It presents the analysis, design and simulation of a three-port integrated isolated Ćuk converter (Fig. 5.1) which uses an active soft-switching method to achieve high efficiency, which is of paramount importance in a multiport interface. The active-clamp technique is utilised with C_r

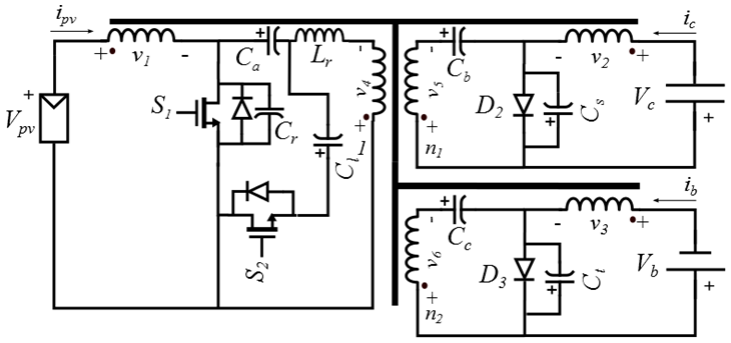

Figure 5.1: ZVS-ZCS Active-Clamp Ćuk Converter with Integrated Magnetics

and L_r to achieve ZVS turn-on of the switches S_1 and S_2 in the active power port. In addition to this, the input and output inductors L_1 and L_2 along with the isolation transformer are integrated into a single magnetic core and the corresponding magnetic circuit is analysed to achieve nearly-zero ripple on the input and output currents. This will reduce the demands on the controller as there will be negligible excursion from the maximum power-point of the PV module. Finally, these devices have reduced voltage and current stresses on the main switch and allow operation at high frequency.

This chapter focuses on the soft-switching scheme. The magnetics design and zero-ripple criteria are assumed from the start and not emphasized here, since the method follows from the preceding chapters.

5.2 Soft-Switching Mechanism

To simplify the analysis, the input and output currents are assumed to be pure dc (the integrated magnetic structure aids in this approximation and removes the need for bulky inductors as in [60]). The energy transfer capacitors C_a, C_b, C_l, the clamp capacitor C_l are also fairly large compared to the snubber capacitors C_r, C_s and C_t, hence they can be assumed as fixed voltage sources.

The six main stages of the active-clamp converter are shown in Fig. 5.2 and the expected theoretical waveforms are shown in Fig. 5.3. The switching cycle starts at $t = 0$, when switch S_1 is turned off. The capacitor C_r is now charged under a constant current of $I_{pv} + n_1 I_g + n_2 I_b$.

The charging operation of C_r continues until $v_{C_r} = V_{pv} + \frac{V_b}{n_2} = V_{pv} + \frac{V_c}{n_1}$. (In this

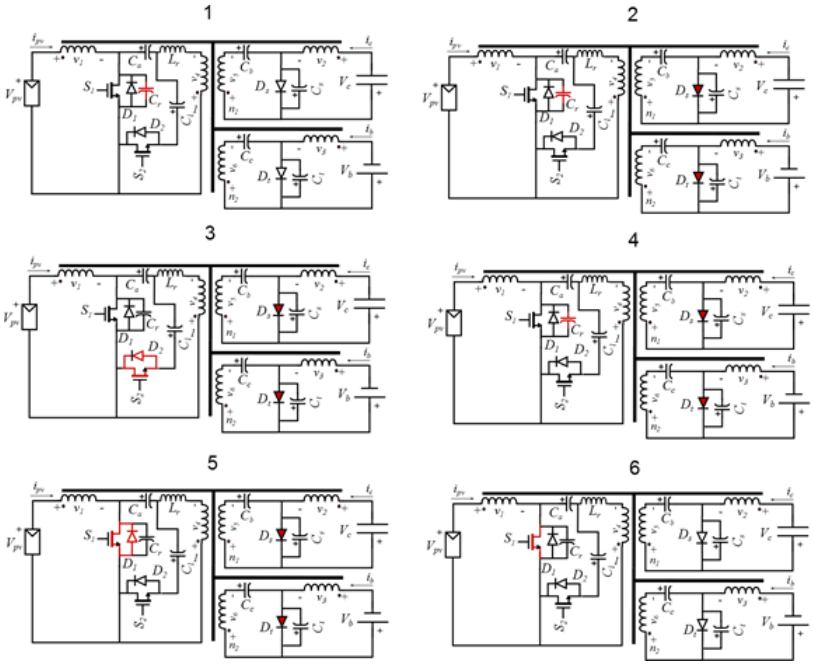

Figure 5.2: ZVS-ZCS Intervals

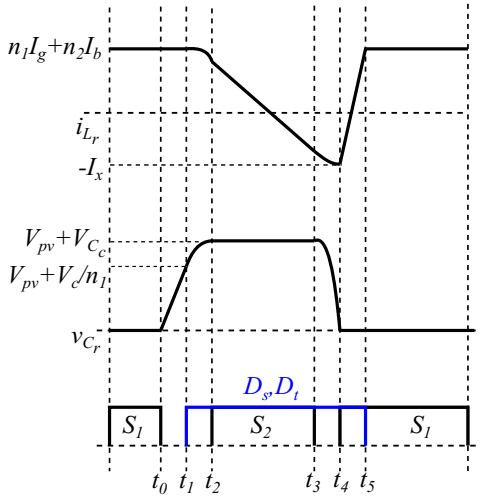

Figure 5.3: Theoretical Waveforms of the proposed Ćuk Converter

converter, the output voltages V_c and V_b are tightly regulated and are proportional, i.e., $\frac{V_c}{n_1} = \frac{V_b}{n_2}$ because of the coupled 6-winding magnetic structure.) This happens at $t = t_1$, when D_s and D_t turn on. In the next interval, L_r and C_r undergo resonance until $v_{C_r} = V_{pv} + V_{C_l}$ at $t = t_2$, when the antiparallel diode of S_2 becomes forward-biased. At this moment, S_2 can be turned on at zero-voltage. Thus begins the second quasi-steady state of the converter. During this time, the current through L_r ramps down and reverses in direction. It terminates at $t = t_3$, when we turn off S_2. This occurs with ZCS due to the presence of snubber capacitors C_s and C_t on the secondary and tertiary sides. Now C_r is discharged by the reversed current through L_r until it reaches zero voltage at $t = t_4$. S_1 can be turned on at this time at zero-voltage. The voltage across L_r has reversed again and become positive. Thus the current through L_r will now ramp up until it reaches $n_1 I_g + n_2 I_b$, turning D off at $t = t_5$. This returns the circuit to the state same as the beginning.

5.3 Design Considerations and Simulation Results

In order to make the topology work in the way described in Section 5.2, there are several design constraints:

1. $V_{C_l} > \frac{V_c}{n_1} = \frac{V_b}{n_2}$ for diodes D_s and D_t to turn on before the antiparallel diode of S_2. The clamp capacitor V_{C_l} should be precharged to a value higher than $\frac{V_c}{n_1}$ by an auxiliary circuit.

2. Since the voltage across C_l is fixed, $\int_0^{T_s} i_{C_l}\, \mathrm{d}t = 0$. This gives $V_{C_l} \sim \frac{2(I_{pv}+n_1 I_g+n_2 I_b)L_r}{(1-D)T_s}$.

3. For $t_2 > t_1$ in Fig.3,i.e., for quasi-resonance to occur in the desired way, we must have $L_r C_r \leq \frac{1}{400\pi^2 {f_s}^2}$. This along with points (2) and (1) give us design equations for L_r and C_r.

4. Timing delay between S_1 turn-off and S_2 turn-on : $t_d \geq \dfrac{\frac{\pi}{2} + tan^{-1}\left(\frac{2\pi f_s L_r (I_{pv}+n_1 I_g+n_2 I_b)}{V_{pv}+V_{C_l}}\right)}{2\pi f_s}$

The proposed converter was simulated with the following specifications : P_o = 250W,V_{pv} = 30V,V_c=400V, V_b=240V, n_1=13, n_2=8. The parameters of the designed circuit were:

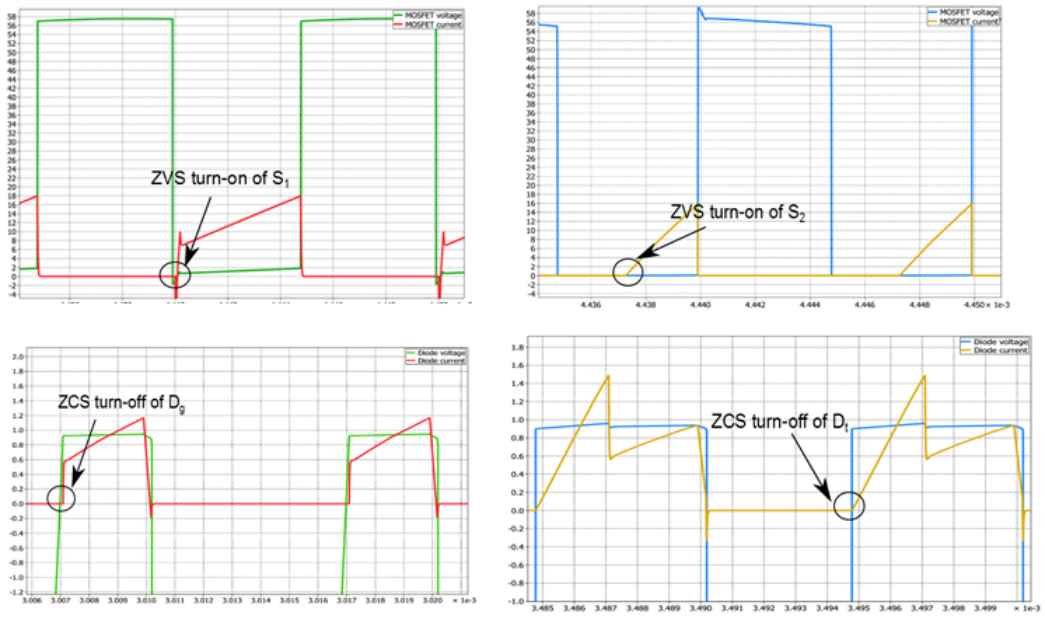

Figure 5.4: (a) ZVS turn-on of S_1 (b) zoomed plot showing ZCS turn-off of S_1 (c) ZVS turn-off of S_2 (d) zoomed plot showing ZCS turn-off of S_2

$C_r = 1nF$	$C_s = 2nF$
$C_l = 100\mu F$	$C_t = 2nF$
$L_r = 0.625\mu H$	$L_r = 0.625\mu H$
$R_c = 1216\Omega$	$R_b = 461\Omega$

Resistances R_c and R_b were chosen to emulate the grid port and battery port currents respectively. The important waveforms demonstrating the soft-switching capability of this topology are shown in Fig. 5.4. The waveforms relating to L_r current C_r voltage are also shown in Fig. 5.5, which confirm the expected theoretical waveforms.

Fig. 5.6 shows that the input current has significantly larger ripple content (15% peak-to-peak) now compared to the non soft-switching topology discussed in [17]. The grid and battery currents have lower ripple content (10% peak-to-peak) compared to the input (PV) current, however, it is still much larger than the corresponding values discussed in [17]. This trade-off is due to the fact that the ZVS-ZCS components on the input side of the isolation transformer cause loss of symmetry of the circuit and the proportionality of the magnetic winding voltage waveforms is somewhat destroyed.

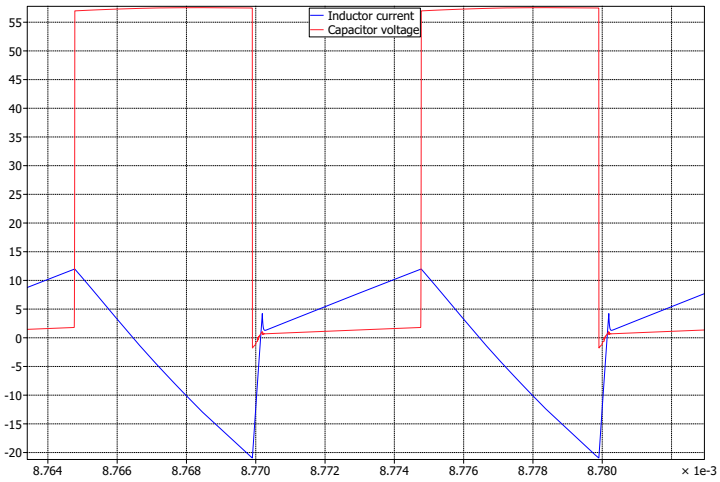

Figure 5.5: Current in L_r and Voltage in C_r

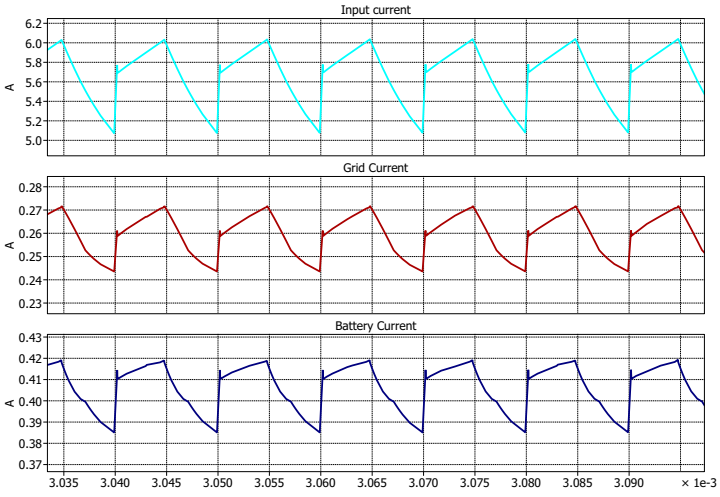

Figure 5.6: Input and Output currents

However, we gain in terms of efficiency of the converter due to the soft-switching features. Hence, depending on the requirement, the appropriate topology can be chosen. If the requirement is lower Electromagnetic Interference (EMI), we choose [17], while if the requirement is higher efficiency, we choose this topology.

Chapter 6

A Modified Three-Port Ćuk Converter with Zero Ripple Terminal Currents on Two Ports and Independent Regulation of Output ports

6.1 Introduction

Renewable integration presents several challenges in terms of improvement of the power electronic interface. Traditionally, three different dc-dc converters would have been used for PV, load and the battery. Hence the availability of a suitable multiport DC-DC converter for a microgrid that can meet the requirements of high efficiency, modularity, low component count, ease of regulation, is of paramount importance.

The main contribution of this chapter is to propose a non-isolated three-port dc/dc converter that is capable of interfacing with a PV port, a battery port and a super-capacitor port. The converter is derived from the parent Ćuk topology, and is built around a partially integrated magnetic core and the addition of an extra bidirectional switch. The features of the converter include: 1) zero fundamental ripple currents on two ports (PV and Battery), 2) CCM operation of the PV and Battery port and DCM operation of the supercapacitor port, 3) Bidirectional power flow at supercapacitor and

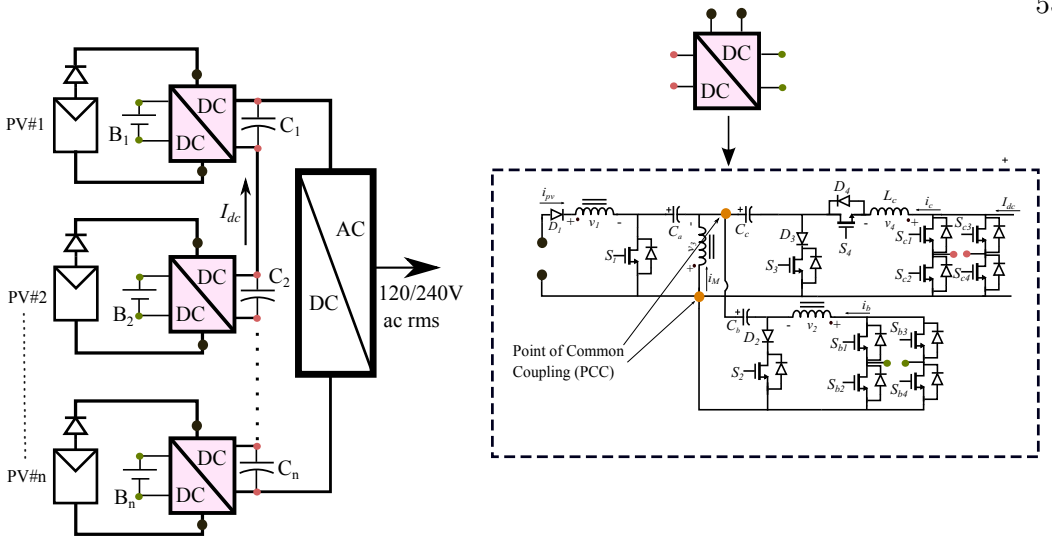

Figure 6.1: Application and Proposed Topology

battery ports, 4) Independent regulation of battery and supercapacitor ports, and 5) Step-up/step-down dc-dc conversion. The converter is non-isolated and can be made extremely compact with the use of wide band-gap devices and planar magnetics. As such, it is an ideal candidate for the application described in Fig. 1): A storage augmented modular microconverter for interfacing to a grid-tied inverter. $B_1, B_2, ...B_n$ are batteries which represent distributed storage while $C_1, C_2, ...C_n$ are supercapacitors which can tolerate high current ripple and some amount of voltage fluctuation. Since supercapacitors are normally not available for high voltage ratings, stacking them up in series as in Fig. 6.1 can generate a high dc-bus voltage for the inverter to work with. The connection terminals are showed by means of appropriately colored dots. The proposed DC-DC converter is tasked with power management between each PV module and its corresponding supercapacitor and battery, which includes battery charging/discharging and maximum power point tracking (MPPT) operation of the PV panel as is necessary in appropriate modes of operation. The supercapacitor voltage is allowed to float at a value required by the central DC-AC inverter. It is the job of the DC-AC inverter to regulate the DC bus voltage [57], i.e., the sum of the voltages on $C_1, C_2, ...C_n$. Additionally, the proposed topology can also be a candidate for a power management system in a futuristic application like a solar vehicle with hybrid battery/supercapacitor energy storage. However, it is to be noted that this converter is not proposed as a dual-input

converter, i.e., we cannot have the following scenarios:(i) PV and supercapacitor port simultaneously charging the battery, (ii) PV and battery simultaneously feeding power into the supercapacitor/grid port. This happens because with varying nominal voltages at two ports feeding power, there can be competing voltages driven at the point of common coupling from the two input sources.

The rest of the chapter is organized as follows. Section 5.2 describes the motivation and steps involved in the development of the converter and theoretical waveforms. Section 5.3 deals with the magnetics design. Section 5.4 talks about the various power modes. Section 5.5 describes the simulation results while Section VI deals with experimental results.

6.2 Converter Description

The original motivation for a multiport converter was a completely integrated magnetic three-port Ćuk converter as proposed in our earlier work [46]. However, although it offered zero fundamental ripple currents on all three ports, it also suffered from a drawback in terms of the application proposed in this paper. This was due to the fact that the voltages on the output ports were tightly coupled, which is a direct consequence of the zero-ripple condition which requires all the magnetic winding voltages to be proportional [45]. The onus is to decouple the grid/supercapacitor port voltage from the battery port voltage so as to let it be regulated by the inverter stage [57], while still maintaining zero-ripple currents on the PV and battery terminals. The grid port can sink a significant amount of current ripple, due to the presence of the large dc-bus capacitor [33] and hence the zero-ripple requirement can be relaxed for this terminal of the three-port interface. This is achieved with the addition of the extra diode D_4 to force the current through L_c into DCM. In the original uncoupled topology, all the ports simultaneously go into CCM or DCM when the sum of all the terminal inductor currents goes to zero [45]. With a completely integrated magnetic structure, all the port inductor currents are zero-ripple and obviously in CCM for any steady-state. By breaking the magnetic structure into a three-winding coupled inductor (represented by the three self-inductances L_{pv}, L_M, L_b and a single inductor L_c as shown in Fig. 6.2, L_g no longer has voltage waveforms across it which are proportional to the voltages across the other magnetic windings. The converter is also made bidirectional at the battery and supercapacitor ports by addition of switches $S_2, S_3, S_{b1}, S_{b2}, S_{b3}, S_{b4}, S_{c1}, S_{c2}, S_{c3}, S_{c4}$ and D_4

Table 6.1: Converter Operation Modes

Switch	Mode I	Mode II	Mode III
S_1	PWM	OFF	OFF
D_1	ON	OFF	OFF
S_2	ON	ON	PWM
D_2	PWM	PWM	PWM
S_3	ON	PWM	ON
D_3	PWM	PWM	PWM
S_4	PWM	ON	OFF
D_4	PWM	ON	OFF
S_{b1}	ON	ON	OFF
S_{b2}	OFF	OFF	ON
S_{b3}	OFF	OFF	ON
S_{b4}	ON	ON	OFF
S_{c1}	ON	OFF	ON
S_{c2}	OFF	ON	OFF
S_{c3}	OFF	ON	OFF
S_{c4}	ON	OFF	ON

(marked in red in Fig. 6.2). Please note that none of the labelled switches in Fig. 6.2 represent body diodes.

6.2.1 Mode I : PV to Supercapacitor and Battery

The PWM waveforms for this mode are shown in Fig. 6.3. Interval 1 denotes the time interval when PWM switch S_1 is on. At $t = DT_S$, S_1 is turned off. The diodes D_2 and D_3 turn on simultaneously at this time to conduct i_c and i_b respectively. The input current i_{pv} is divided between diodes D_2 and D_3. The branch consisting of L_M carries the ripple current of the L_{pv} and L_b. There is no dc current flowing through L_M. At $t = D_2T_s$, the current through L_c goes to zero and the supercapacitor port enters DCM, thereby commencing the start of the final interval 3. In order to find out the steady-state dc voltages across the energy transfer capacitors C_a, C_b and C_c, consider the following:

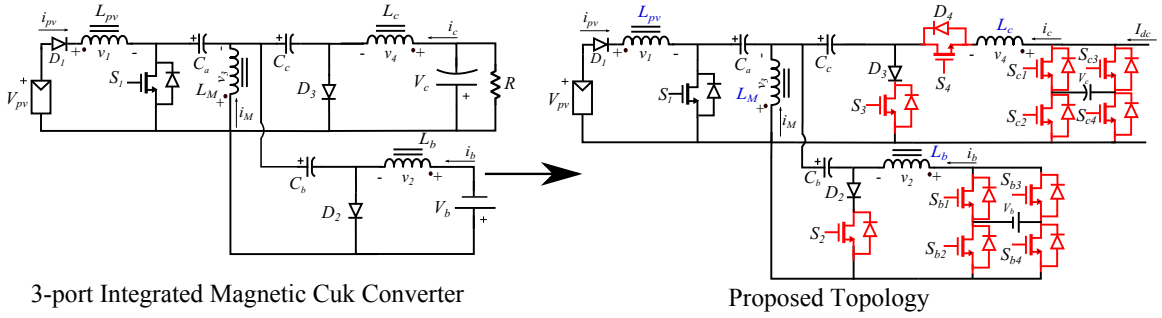

Figure 6.2: Evolution of Proposed Topology

- From Kirchoff's voltage law (KVL) around the input loop consisting of V_{pv}, D_1, L_{pv}, C_a and L_M, $v_{C_a} = V_{pv}$.
- From KVL around the output loop consisting of V_b, L_b, C_b and L_M, $v_{C_b} = V_b$.
- Since D_2 and D_3 turn on at $t = DT_s$, from KVL around C_c, D_3, L_M, C_b and $D_2, v_{C_c} = v_{C_b} = V_b$.

We now derive the converter steady-state voltage conversion ratios for the two ports. From volt-sec balance on L_c, we have the average voltage

$$< v_{L_c} >= 0 \implies \frac{V_c}{V_{pv} + V_b - V_c} = \frac{D}{D_2} \tag{6.1}$$

The average current through L_c is

$$< i_c >= I_c = \frac{V_c}{R} = \frac{\Delta i_c (D + D_2)}{2} \tag{6.2}$$

where Δi_c is the peak-to-peak current ripple in L_c and R is the load resistance which models the dc current that flows into the dc bus capacitor of the DC-AC inverter at the supercapacitor port. Application of positive volt-seconds during interval 1 gives

$$\Delta i_c = \frac{V_{pv} D T_s}{L_c} \tag{6.3}$$

From the CCM voltage conversion ratio between the PV port and the battery port, we have

$$V_b = \frac{D V_{pv}}{1 - D} \tag{6.4}$$

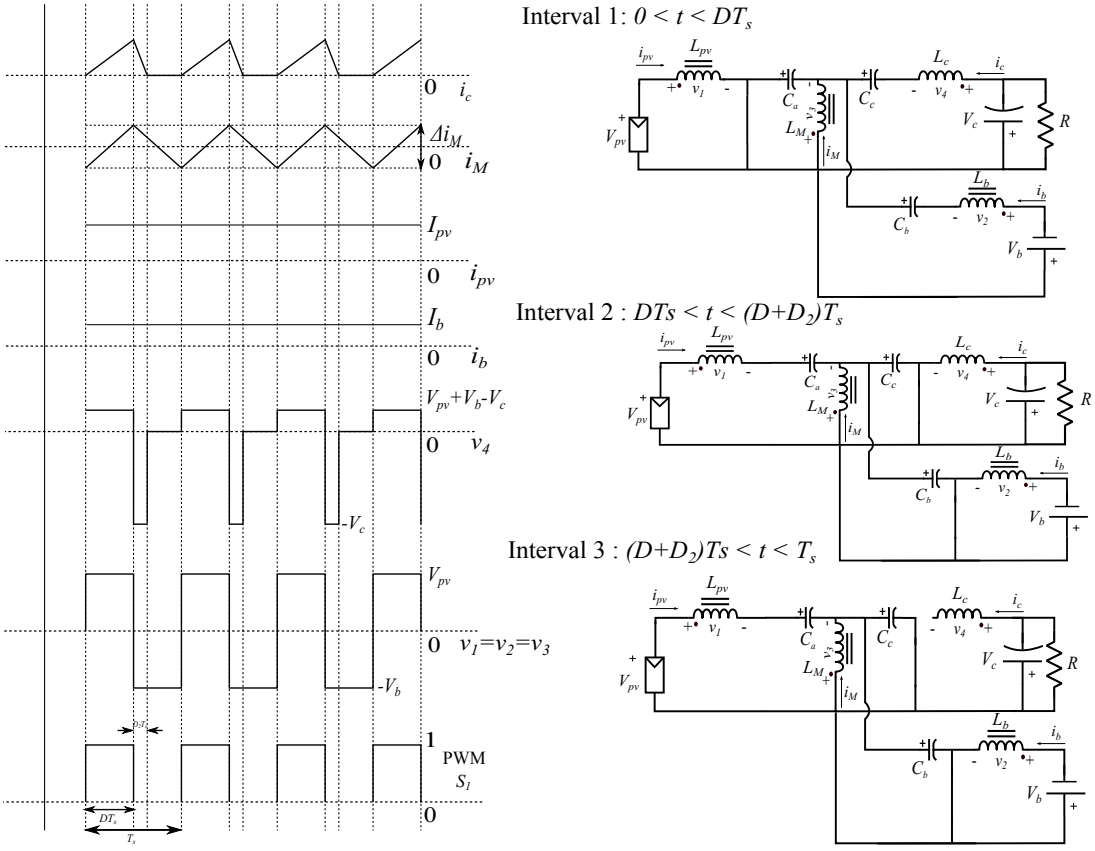

Figure 6.3: PWM intervals and waveforms (Mode I)

Solving (1)-(4), we have

$$V_c = DV_{pv}\sqrt{\frac{RT_S}{(1-D)L_c}} \tag{6.5}$$

6.2.2 Mode II : Supercapacitor to Battery

In this mode, the polarity of the supercapacitor terminal is reversed by turning on S_{c2}, S_{c3} and turning off S_{c1}, S_{c4}. Turning off S_1 prevents any kind of current flow in the direction of the PV terminal (also aided by D_1). The converter is made to operate in CCM by keeping S_4 on all the time, similar to a conventional Ćuk converter. This is because we would like to have duty-ratio control of the battery port while charging it from a supercapacitor, which now behaves as the input port. The voltages across all the windings are proportional as shown in Fig. 6.4. There are two distinct PWM intervals. Due to the integrated magnetics design, the ac ripple in the battery current is shifted to L_M, making the battery current ripple free. The CCM conversion ratio between the supercapacitor and battery is given by:

$$V_b = \frac{DV_c}{1-D} \tag{6.6}$$

6.2.3 Mode III : Battery to Supercapacitor

In this mode, the polarity of the supercapacitor terminal is reversed by turning on S_{b2}, S_{b3} and turning off S_{b1}, S_{b4}. Turning off S_1 prevents any kind of current flow in the direction of the PV terminal (also aided by D_1). Since the supercapacitor port is driven here by the battery port, it is more likely for this port to operate in DCM. There are three PWM intervals as shown in Fig. 6.5. Due to the integrated magnetics design, the ac ripple in the battery current is shifted to L_M, making the battery current ripple free (refer Fig. 6.5), although the shape of i_M changes to discontinuous here. The DCM conversion ratio between the battery and supercapacitor is derived below. The peak-to-peak ripple in i_c is given by:

$$\Delta i_c = \frac{(V_b + V_{C_b} - V_c)DT_s}{L_c} \tag{6.7}$$

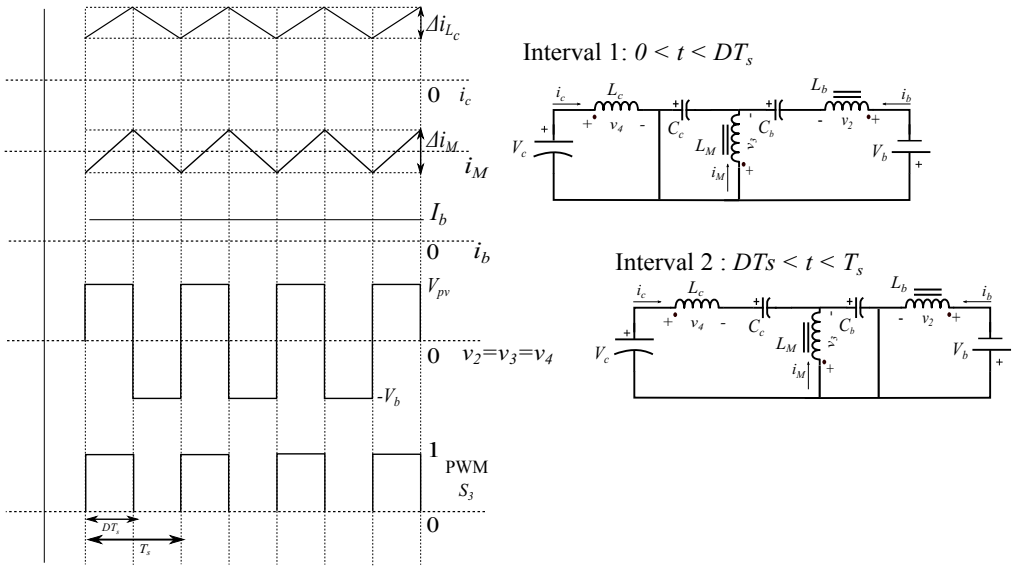

Figure 6.4: PWM intervals and waveforms (Mode II)

and

$$\Delta i_c = \frac{V_c D_2 T_s}{L_c} \tag{6.8}$$

Also in DCM, the following holds:

$$\frac{\Delta i_c}{2}(D + D_2)T_s = \frac{V_c}{R} \tag{6.9}$$

The final condition is

$$\frac{1}{T_s}\int_0^{T_s} i_{C_c} dt = 0 \tag{6.10}$$

where

$$i_{C_c} = \begin{cases} -i_c & \text{if } 0 < t < DT_s \\ I_b & \text{if } DT_s < t < (D + D_2)T_s \\ 0 & \text{if } (D + D_2)T_s < t < T_s \end{cases} \tag{6.11}$$

Using (11) in (10) yields

$$V_b + V_{C_b} - V_c = \frac{2D_2 I_b L_c}{DT_s} \tag{6.12}$$

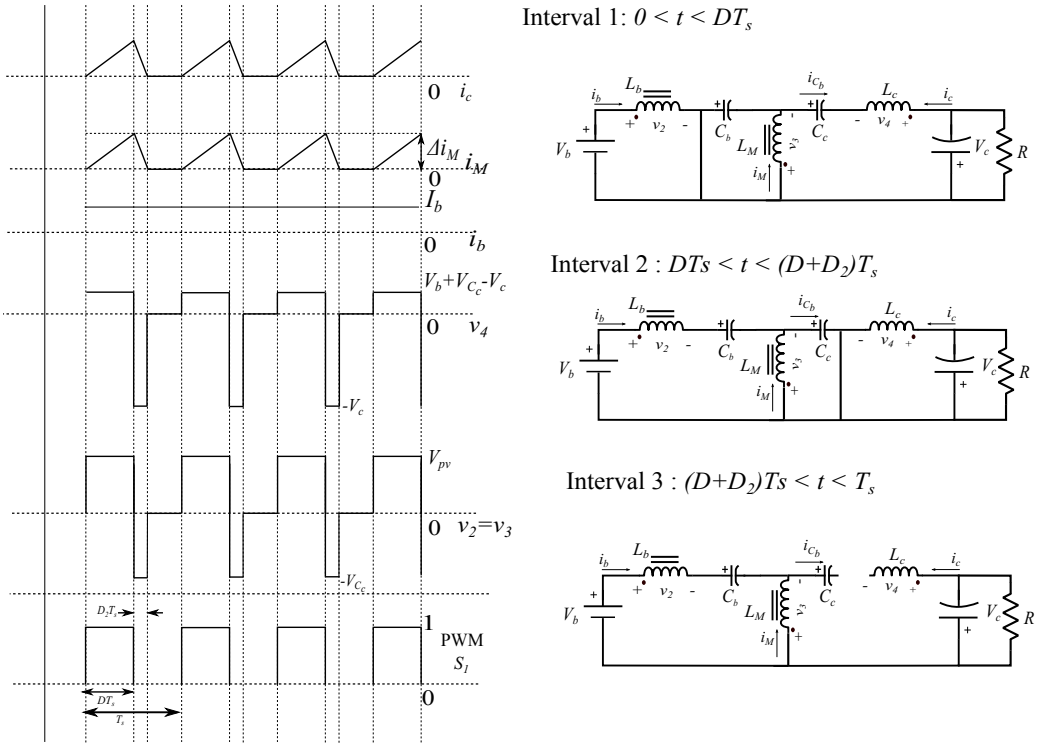

Figure 6.5: PWM intervals and waveforms (Mode III)

From (7) & (8) we get

$$(V_b + V_{C_b} - V_c)D = V_c D_2 \tag{6.13}$$

Using (13) in (12),

$$V_c = \frac{2L_c I_b}{DT_s} \tag{6.14}$$

Assuming the converter to be ideal, i.e. $V_b I_b = \frac{V_c^2}{R}$, the final voltage conversion ratio in DCM is given by

$$\frac{V_c}{V_b} = \frac{DRT_s}{2L_c} \tag{6.15}$$

6.3 Magnetics Design

Having established the basic operation of the converter in the various modes, we now describe the design procedure of the magnetic components, which is an integral part of the converter.

6.3.1 Design of the three-winding coupled inductor

This design procedure is adopted in many ways from our earlier work in [48]. The three-winding coupled inductor structure can be described in terms of the following equations:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{12} & L_{22} & L_{23} \\ L_{13} & L_{23} & L_{33} \end{bmatrix} \times \frac{d}{dt} \begin{bmatrix} i_{pv} \\ i_b \\ i_M \end{bmatrix} \tag{6.16}$$

where L_{jj} = self-inductance of j^{th} winding, L_{jk} = mutual inductance between j^{th} and k^{th} winding ($j \neq k$), and $j, k \in \{1, 2, 3\}$. L_{11} corresponds to L_{pv}, L_{22} corresponds to L_b and L_{33} to L_M.

The voltages v_1, v_2, v_3 are proportional to each other [45]. Hence we have $v_1 = v_2 = v_3$. For zero-ripple in i_{pv} and i_b, their time derivatives must be zero at all times. This provides the following analytical condition for the inductances defined in (8):

$$L_{13} = L_{23} = L_{33} \tag{6.17}$$

Although achieving these conditions in the inductances is the end goal, they are not very helpful in the actual magnetic design process. We need a core structure and a method to do an approximate design which gives us the winding turns and conductor dimensions for each winding. This is explained in the next section. Once the core size and the winding sizes and turns are known, we can use Finite-Element-Modelling (FEM) methods to obtain the right air-gap and the correct design.

The Area-Product Method[48, 49] is modified from its classical inductor design counterpart in to design this 3-winding coupled inductor structure. The formulation of the Area-Product requires consideration of the following:

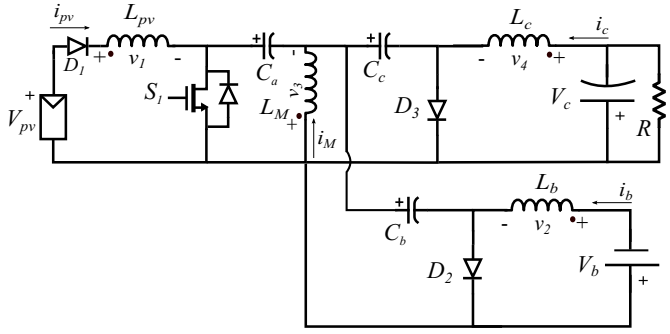

Figure 6.6: Uncoupled Ćuk converter

Magnetizing Inductor

The basic idea for zero-ripple is to shift the current ripple in windings 1 & 2 (PV and Battery inductors) to the "magnetizing" inductor (winding 3) via a coupled magnetic pathway as explained by Ćuk in [51]. For this purpose, initially we consider that the input and output inductors are kept separate from the magnetizing inductor in an uncoupled Ćuk converter as in Fig. 6.6, and we designed the input and output inductors according to their ripple specification (same for both), for the peak-to-peak ripple in each, we would have:

$$\Delta i_{L_{pv}} = f_r I_{pv} \tag{6.18}$$

$$\Delta i_{L_b} = f_r I_{b,max} \tag{6.19}$$

where f_r = fraction of dc value of the corresponding inductor currents, and I_{pv} and I_b are the dc values of the currents through windings 1 and 2 respectively. If the peak-to-peak ripple in magnetizing current is Δi_M, due to the ripple steering effect [18] in the coupled inductor, we have

$$\Delta i_M = \Delta i_{L_{pv}} + \Delta i_{L_b} = f_r(I_{pv} + I_b) \tag{6.20}$$

The coupled inductor is designed assuming that the full rated power of the converter flows through the battery port, i.e., the supercapacitor port is inactive. Then for a fully-efficient Ćuk converter,

$$I_{b,max} = \frac{I_{pv}(1-D)}{D} \quad \text{where} \quad D \quad = \text{duty-ratio of } S_1 \tag{6.21}$$

During the interval when S_1 is on, a voltage of V_{pv} is applied across the magnetizing inductor, since the steady state voltage across C_a (Fig. 6.1) is V_{pv}. This gives:

$$\Delta i_M = \frac{V_{pv} D}{L_p f_s} \tag{6.22}$$

where f_s = switching frequency, L_p = isolation transformer magnetizing inductance. From (12)-(13) we have

$$\Delta i_M = \frac{f_r I_{pv}}{D} \tag{6.23}$$

From (14) and (15), then

$$L_M = \frac{D^2 Z_{pv}}{f_r f_s} \quad (Z_{pv} = \text{PV source impedance}) \tag{6.24}$$

Since the converter will operate at the maximum power point of the PV panel for maximum utilization, it seems reasonable to pick

$$L_M = \frac{D_{max}^2 Z_{MPP}}{f_r f_s} \tag{6.25}$$

where $Z_{MPP} = Z_{pv}$ at maximum power point. For a PV panel, the stable region of operation is to the right of the maximum power point (MPP) on the P-V curve. Since the grid voltage is asssumed to be constant throughout, operation at maximum duty ratio of a Ćuk converter corresponds to the MPP (hence $D_{MPP} = D_{max}$).

Core Structure, Zero-ripple and Peak Flux Density

An EE-core with the same air gap across all the limbs is chosen for symmetry reasons and tunability as explained in [45]. The windings are placed as shown in Fig. 6.7. At very low air-gap, the inductances vary rapidly and the design point is not suited for the zero fundamental ripple current condition on windings 1 & 3. The corresponding flux-reluctance circuit is obtained by removing several negligible leakage flux components and clubbing together the others similar to [45]. The reluctances are defined in terms of a reluctance parameter $\mathcal{R}$, where

$$\mathcal{R} = \frac{2x}{\mu_0 A_c} \quad (\frac{x}{2} = \text{spacer airgap}) \tag{6.26}$$

$\mathcal{R}/2$ and $\mathcal{R}/4$ represent the reluctances due to air-gap in the three limbs, while

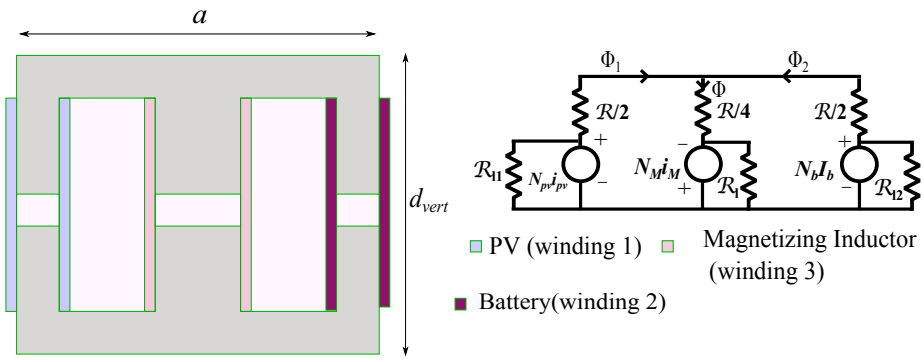

Figure 6.7: Core Structure and Flux Reluctance Model

$\mathcal{R}_l$, $\mathcal{R}_{l1}$ and $\mathcal{R}_{l2}$ represent those due to leakage as shown in Fig. 6.7. The zero-ripple condition derived in [53] dictates that:

$$\frac{N_{pv}}{N_M} = 2 + \frac{x}{l} = f \tag{6.27}$$

where l = "leakage parameter"[45]. The leakage parameter has the dimensions of length and models the center limb leakage flux path, i.e., $\mathcal{R}_l = \frac{l}{\mu_0 A_c}$. '$f$' is a turns ratio which is later used in deriving the area product.
N_{pv} = No. of turns of winding 1, N_M = No. of turns of winding 3, N_b = No. of turns of winding 2. N_{pv} is chosen equal to N_b to simplify the design.

Applying KCL and KVL to the magnetic circuit of Fig. 6.7 yields:

$$N_{pv}i_{pv} + \phi_1\frac{\mathcal{R}}{2} + \phi\frac{\mathcal{R}}{4} + N_M i_M = 0 \tag{6.28}$$

$$N_b i_b + \phi_2\frac{\mathcal{R}}{2} + \phi\frac{\mathcal{R}}{4} + N_M i_M = 0 \tag{6.29}$$

$$\phi = \phi_1 + \phi_2 \tag{6.30}$$

Solving (28)-(30) for ϕ_1, ϕ_2 and ϕ yields the following equations:

$$\phi_1 = \frac{1.5N_{pv}i_{pv} - 0.5N_b i_b + N_M i_M}{\mathcal{R}} \tag{6.31}$$

$$\phi_2 = \frac{1.5N_b i_b - 0.5N_{pv}i_{pv} + N_M i_M}{\mathcal{R}} \tag{6.32}$$

$$\phi = \frac{N_{pv}i_{pv} + N_b i_b + 2(N_M i_M)}{\mathcal{R}} \tag{6.33}$$

Peak flux densities are needed to in order to find the correct winding area A_c. To find them, we assume :

- i_{pv} and i_b are purely dc, i.e., $< i_{pv} >= i_{pv,rms} = I_{pv}$, $< i_b >= i_{b,rms} = I_b$
- The converter is 100% efficient: $V_{pv}I_{pv} = V_cI_c + V_bI_b$.
- $\frac{V_b}{V_{pv}} = \frac{D}{1-D}$. This equation ceases to be valid beyond $D > 0.75$ due to the influence of parasitic resistances.

Let us define $r_p = \frac{V_bI_b}{V_{pv}I_{pv}}$. Thus $0 < r_p < 1$. Using the above assumptions, we can show that (Refer Appendix A) at quasi-steady state the peak flux densities corresponding to ϕ_2, ϕ_1, ϕ are

$$\hat{B_1} = \frac{N_{pv}I_{pv}f_{\phi_1}(D, r_p) + 2 * max(N_Mi_M)}{\mathcal{R}A_c} \quad \text{where} \quad f_{\phi_1}(D, r_p) = 3 - \frac{(1-D)r_p}{D} \tag{6.34}$$

$$\hat{B_2} = \frac{N_{pv}I_{pv}f_{\phi_2}(D, r_p) + 2 * max(N_Mi_M)}{\mathcal{R}A_c} \quad \text{where} \quad f_{\phi_2}(D, r_p) = \frac{3r_p(1-D)}{D} - 1 \tag{6.35}$$

$$\hat{B} = \frac{N_{pv}I_{pv}f_{\phi}(D, r_p) + 2 * max(N_Mi_M)}{\mathcal{R}A_c} \quad \text{where} \quad f_{\phi}(D, r_p) = 1 + \frac{r_p(1-D)}{D} \tag{6.36}$$

The second term in the above three expressions is common for all the three limbs. Assuming that the converter operates close to the MPP of the PV panel, the quantity $N_{pv}I_{pv}$ is fairly constant. Therefore, the unitless quantities f_{ϕ_2}, f_{ϕ_1} and f_{ϕ} decide the peak flux densities in the core. These functions are plotted in Fig. 6.8. It is seen that the limb with winding 2 has the most flux density for $D <= 0.5$ while the limb with winding 1 has the most flux density for $D >= 0.5$. The absolute maximum flux density across the three limbs of the core is $B_{peak} = \hat{B}_{\phi_2}|_{D=0.3}$ for $D \in (0.3, 0.75)$.

Window Area

Windings 1 & 3 are in the left window of the EE-core while windings 2 & 3 are in the right window as shown in Fig. 6.9. Using equation (19), the window area can be expressed as (k_{Cu} is the fill factor and J_{rms} is the current density in all the windings)

$$A_{w1} = \frac{N_{pv}I_{pv} + N_Mi_{M,rms}}{k_{Cu}J_{rms}} = \frac{a_{w1}fN_MI_{pv} + N_Mi_{M,rms}}{k_{Cu}J_{rms}} \tag{6.37}$$

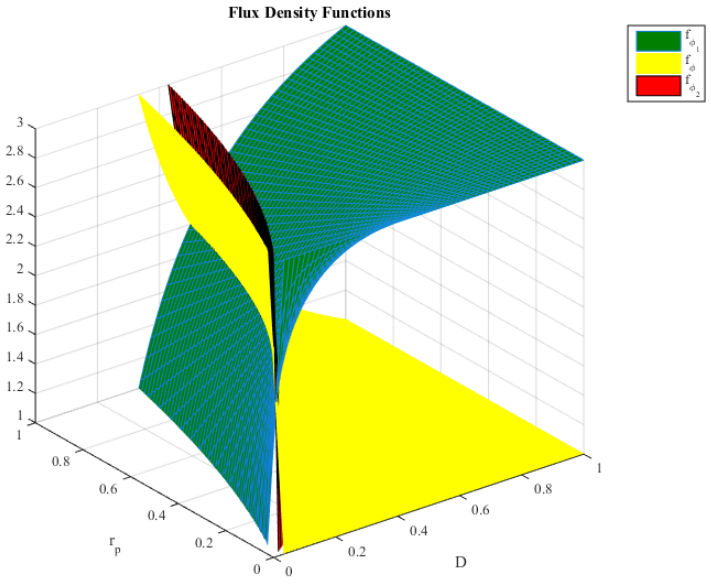

Figure 6.8: Determination of max. flux density

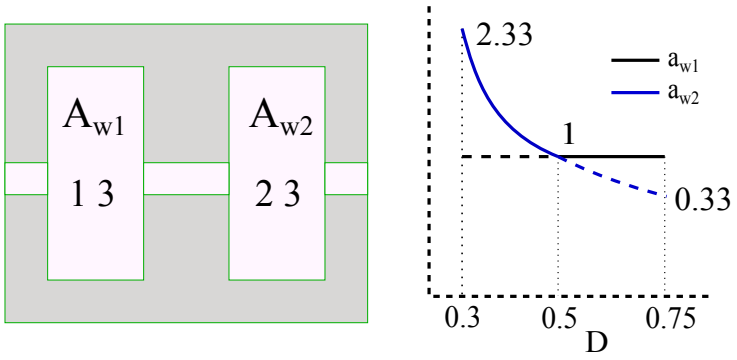

Figure 6.9: Window Area Determination ($r_p = 1$)

if the left window is used to design the core, and

$$A_{w2} = \frac{N_b I_b + N_M i_{M,rms}}{k_{Cu} J_{rms}} = \frac{a_{w2} f N_M I_{pv} + N_M i_{M,rms}}{k_{Cu} J_{rms}} \tag{6.38}$$

if the right window is used to design the core. Using the definition of r_p, (13) and (19), we obtain $a_{w1} = 1$ and $a_{w2} = \frac{r_p(1-D)}{D}$. It is evident that a_{w1} and a_{w2} decide which

window area is larger and at what duty ratio. These are plotted in Fig. 6.9 as a function of D, with the worst case value of $r_p = 1$. It is seen that selecting a_{w2} (henceforth A_{w2}) at $D = 0.3$ takes care of the entire design space, since in the actual physical core, both window areas are identical. The final expression is:

$$max(A_w) = A_{w2}|_{D=0.3} = \left(\frac{N_b I_b + N_M i_{M,rms}}{k_{Cu} J_{rms}} \right) \Bigg|_{D=0.3} \tag{6.39}$$

It is seen that the worst cases occur at $D = 0.3$ for both peak flux density and window area. Hence it would be a natural choice to define the worst case area product at this point, as will be demonstrated in the next section.

Area Product

For $D \in (0.3, 0.5)$ we obtain From (27),

$$N_M = \frac{\hat{B_2} A_c \mathcal{R}}{\left(3 - \frac{(1-D) r_p}{D} \right) I_{pv} + 2 * max(i_M)} \tag{6.40}$$

From (30) & (31) (window area),

$$N_M = \frac{A_{w2} k_{Cu} J_{rms}}{\frac{r_p (1-D)}{D} I_{pv} + i_{M,rms}} \tag{6.41}$$

The total core reluctance at sufficiently large air-gap seen by winding 3 can be evaluated to $\mathcal{R}/2$. This is true when $\frac{x}{2} > \frac{10 l_m}{\mu_r}$, where l_m is the mean magnetic path length of the EE core and μ_r is the relative permeability of the Ferrite Core. This condition is derived in Appendix (B). Hence the primary magnetizing inductance is

$$L_M = \frac{2 N_M^2}{\mathcal{R}} \tag{6.42}$$

From (32)-(34), we can deduce the area product:

$$A_p(\text{Area Product}) = A_c A_w = \frac{L_M I \hat{I}}{2 \hat{B} k_{Cu} J_{rms}} \tag{6.43}$$

where $\hat{B} = \hat{B}_2$ for $D \in (0.3, 0.5)$. Also

$$\hat{I} = \left(3 - \frac{(1-D)r_p}{D}\right) I_{pv} + 2 * max(i_M) \tag{6.44}$$

and

$$I = \frac{r_p(1-D)}{D} I_{pv} + i_{M,rms} \quad , \quad i_{M,rms} = \frac{\Delta i_M}{2\sqrt{3}} \tag{6.45}$$

for $D \in (0.3, 0.5)$. Δi_M is the peak-to-peak ripple in the magnetizing inductor current as labelled in Fig. 6.3. It can be seen that A_p is a complex function of D, provided the parameters of the PV panel are provided. The quantities I and $\hat{I}$ reach their maximum at $D = 0.3$, as discussed in the subsections (3) & (4). L_M is calculated in accordance with (17) and is a constant. Hence A_p reaches its maximum at $D = 0.3$.

An iterative design algorithm is outlined in the flowchart of Fig. 10. Once an appropriate core is picked for the worst case design and N_M calculated, the air-gap is computed using an accurate expression of inductance (see Appendix(B)). This is necessary because the inductance varies very rapidly near zero air-gap and the approximate equation (34) is no longer adequate. However, we cannot use the actual equation in formulating the expression of area product because it requires knowledge of the mean magnetic length and core permeability, but the core is not yet known to us. The validity of the design is therefore verified by the condition $g = \frac{x}{2} < \frac{10 l_m}{\mu_r}$. If this condition is satisfied, it means the approximate equation (34) is valid and hence so is the area product expression. Additionally, the ratio N_{pv}/N_M needs to be fairly accurate, i.e., 2.25, hence the minimum integer value for N_M needs to be 4 in order to have integer number of turns on all the four windings. If either of these two conditions are violated, N_M needs to be increased from the intial value N_{M0}. However, now there is the additional problem that the windings will no longer fit in the core window according to (29)-(30). Hence a custom version of the original core with the same area product, but with a more skewed aspect ratio is needed as shown in the flowchart of Fig. 6.10.

6.3.2 Design of the DCM port inductor L_c

The supercapacitor port will operate in DCM for all value of I_c. This condition is given by:

$$\Delta i_c > 2 I_{c,max} \tag{6.46}$$

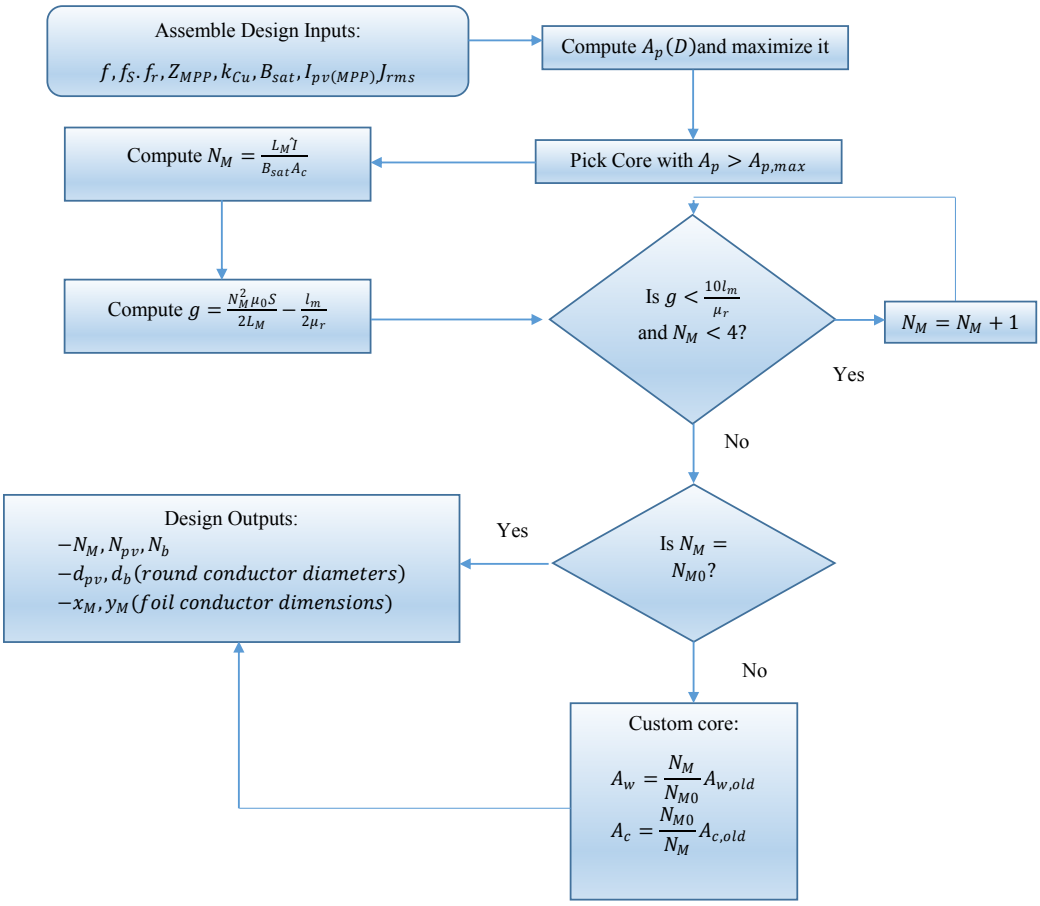

Figure 6.10: Core Selection and Winding Design Flowchart

Using (2)-(3), this can be simplified to

$$L_c < \frac{D_{min} V_{pv}}{2 I_{c,max} f_s} \tag{6.47}$$

6.3.3 Converter Specifications and Design Process

The specifications for the SW 270 mono panel [56], and other relevant design parameters chosen were:

The material used is the 3C94 power ferrite available from Ferroxcube. The Ferrite is designed for use up to 300 kHz, beyond which core losses become significant. The

Table 6.2: Converter Specifications

f_r	Z_{MPP}	f_S	I_{pv}	J_{rms}	B_{sat}	k_{Cu}	μ_r	f
0.6	3.5 Ω	100 kHz	9.44 A	4 A/mm^2	0.33 T	0.4	1790	2.25

choice of factor f was due to guidelines given in [45]. Please note that although B_{sat} for 3C94 material is specified as 0.47 T in the datasheet, a derating factor of approximately 70%[58] is applied to take into account thermal degradation, which means the actual value of B_{sat} used in the design is 0.33 T.

For windings 1 & 2, since they have very low ripple, skin effect is considered negligible and so initially round conductors are chosen. The winding diameters were calculated using the following equation:

$$d_{pv} = d_b = \sqrt{\frac{4I_{pv}}{\pi J_{rms}}} \tag{6.48}$$

Foil conductor is initially chosen for winding 3 & 4. The skin depth for Copper at 100 kHz is $\delta = 0.2$mm and the layer porosity factor is chosen to be $\eta_s = 0.9$. Then the maximum number of turns per layer is:

$$nl_{M,max} = \left\lfloor \eta_s \sqrt{\frac{4}{\pi}} \frac{l_w}{d_M} \right\rfloor \quad \left(d_M = \sqrt{\frac{4i_{M,rms}}{\pi J_{rms}}} \right) \tag{6.49}$$

Here d_M is the diameter if the magnetizing inductor winding was built with round conductors. l_w is the window height of the selected core, with zero air-gap. These values are used for primary and secondary turns if $d_M < \delta$. Otherwise, turns per layer are given by:

$$nl_M = \frac{\eta_s l_w}{\left\lfloor \frac{\pi d_M^2}{4\delta} \right\rfloor} \tag{6.50}$$

Foil width is given by

$$y_M = \frac{\eta_s l_w}{\lfloor nl_M \rfloor} \tag{6.51}$$

while foil thickness is given by:

$$x_M = \frac{\pi d_M^2}{4 y_M} \tag{6.52}$$

For the given solar panel, the design outputs were obtained with a first pass of the algorithm. The outputs are:

Table 6.3: Design Outputs

N_M	N_{pv}	N_b	d_{pv}	d_b	x_M	y_M	Core
8	18	18	1.7 mm	1.7 mm	0.2 mm	1.1 mm	Ferroxcube E42/21/15

For the actual design shown in Fig. 6.11, we use foil windings in place of the round conductors which are difficult to bend around corners, and litz wires in place of the foil conductor in order to reduce proximity effect because the center winding current has high ripple content. For this particular design, since we have only one layer as per the design algorithm for the center winding, proximity effect is not a concern. For designs with more than a layer, foil conductors significantly reduce converter efficiency since no interleaving is possible as in the case of a transformer [29]. The foil conductors used to make this integrated inductor have dimensions of 0.0065"X0.1076" which are the closest match to the cross-sectional area of the round wires. 40/41 Litz Wire is used to make the magnetizing inductor winding.

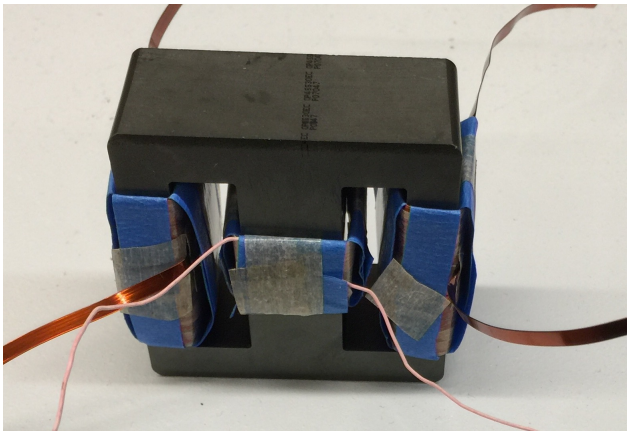

Figure 6.11: Core

Finite Element Modelling : The air-gap is now tuned using Finite-Element-Modelling methods for the zero-ripple condition, similar to [48]. The extracted mutual inductances (L_{13} vs L_{23}), (L_{13} vs L_{33}) as a result of parametric sweeps of the air-gap are shown in Fig. 6.12.

It is seen that the inductances overlap fairly well below g =1 mm. Hence that

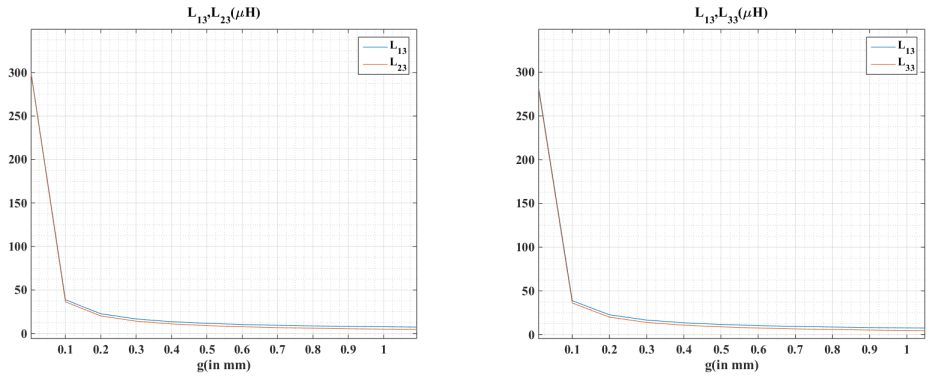

Figure 6.12: plots of the relevant quantities in (2) with FEA

removes the need for an accurate air-gap arrangement. Any no-mex tape with thickness less than 1 mm can used for the spacer air-gap. As for the DCM inductor L_c, a value of 15 μH is chosen for the current set of converter requirements. A Wurth Electronik WE 1541 inductor is used for the same.

6.4 Simulation Results

The proposed modified Ćuk converter is simulated in Pspice. The mutual inductor used in the simulation has the following values:

$$\begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{12} & L_{22} & L_{23} \\ L_{13} & L_{23} & L_{33} \end{bmatrix} = \begin{bmatrix} 47\mu H & 1\mu H & 22\mu H \\ 1\mu H & 47\mu H & 22\mu H \\ 22\mu H & 22\mu H & 22\mu H \end{bmatrix} \tag{6.53}$$

This corresponds to an air-gap of 0.3 mm according to Fig. 6.12. Actual models of devices are used in the simulation. The FET (Field-Effect-Transistor) switches used are the IRFP140N, while the diodes used are Vishay V12P12. Energy transfer capacitors $C_a = C_b = C_c = 47$ μF (Refer Fig.1) are used for simulation. The supercapacitor port is emulated by means of a resistance of 200 Ω while the battery port is emulated by means of a resistance of 10 Ω. A diode-R-C snubber (R=20 Ω, C=20 nF) is used across L_c to dampen oscillations in the current when transitioning to DCM.

The simulation results in PSpice for an input voltage of $V_{pv} = 30$V and $D = 0.5$ are shown in Fig. 6.13 for Mode I. The currents I_{pv} and I_b are low-ripple. The peak-to-peak ripple percentages are 2 and 3 respectively, which is much lesser than the standard ripple

specification of 20% [54]. The output voltages and inductor voltages are also shown. The DCM output voltage is much higher than the CCM output voltage, as expected according to [29].

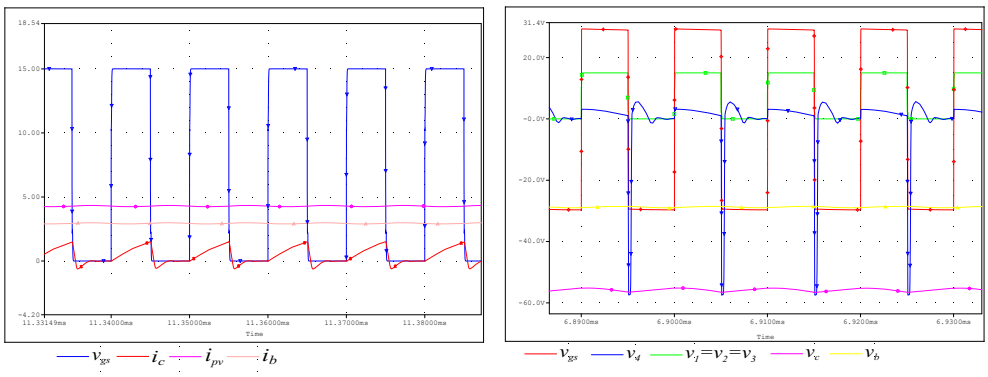

Figure 6.13: Simulated Terminal Currents and Inductor Voltages (Mode I)

Mode II is simulated in Fig. 6.14 for input V_c = 30V and D = 0.5. The ripple in i_c is fairly high, but the conversion ratio is CCM as defined in section II. Mode III is depicted in Fig. 6.15, the results conforming to the waveforms shown in Fig. 6.5, with the addition of parasitic ringing in DCM (damped by the addition of a snubber as discussed earlier).

6.5 Experimental Results

The experimental prototype is shown in Fig. 6.16. Power MOSFETs IRFP140N are used for implementing switches S_1, S_2, S_3 and S_4, while the diodes D_1, D_2, D_3 and D_4 are implemented using V12P12 from Vishay. Gate Drivers IRS2110 are used for feeding PWM signals into S_1, S_2 and S_3 while optoisolator FOD8001 and isolated gate driver FAN7390 are used for S_4.

Table 6.4: Converter Specifications

V_{pv}	R_c	f_S	R_b	D
30V	246 Ω	100 kHz	12.2 Ω	0.5

The Ćuk converter input/output waveforms for the parameters enlisted in Table IV

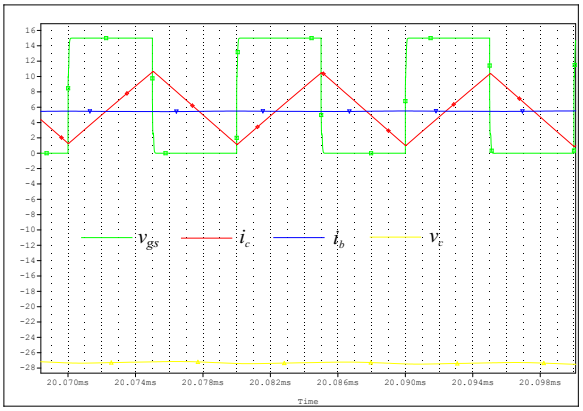

Figure 6.14: Simulated Variables for Mode II

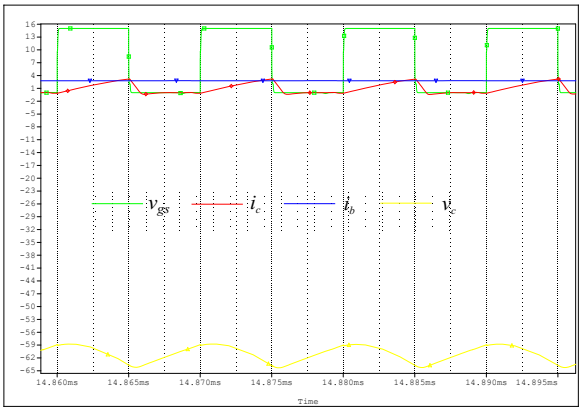

Figure 6.15: Simulated Variables for Mode III

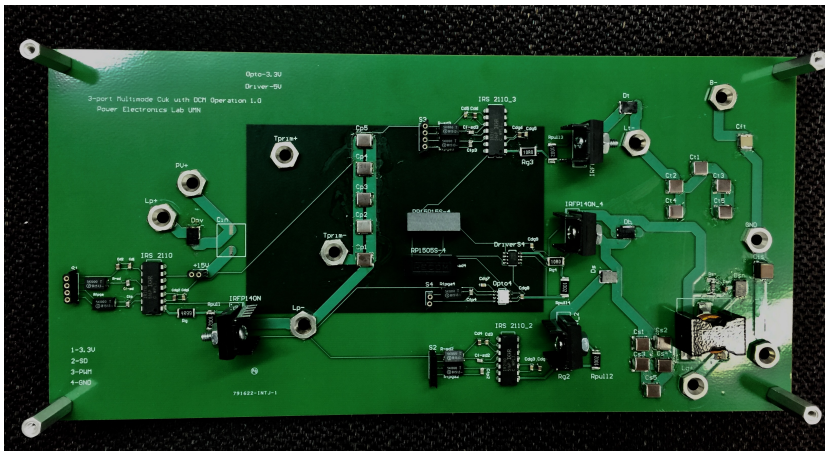

Figure 6.16: Experimental Prototype

are shown for Mode I. Fig. 6.17 shows the currents on the CCM ports, i.e., PV and battery. The input and output current waveforms have very low fundamental ripple content. The ripple values are shown by means of zoomed versions of i_{pv} and i_b in figures 6.18 and 6.19 respectively. This is obtained by using the ac coupling option on the current probes. The peak-to-peak ripple percentage in i_b is 0.066/2.5=2.64% while the peak-to-peak ripple in i_{pv} is 0.1/3=3.33% which is far below the prescribed limit in [27]. The DCM inductor current and voltage are shown in figure 6.20 and a zoomed version of the current is shown in 6.21. The voltage v_{L_c} has a small positive value when S_1 is on, then a large negative value when diodes D_2 and D_3 conduct and finally zero for the rest of the PWM interval, similar to Fig. 6.3. The current decay interval is rather small and there is the expected parasitic ringing when the inductor current is zero. The experimental efficiency is calculated using the following formula:

$$\eta = \frac{\frac{V_b^2}{R_b} + \frac{V_c^2}{R_c}}{V_{pv} I_{pv}}$$

A couple of curves are shown in Figures 6.22. The efficiency tends to be greater when the converter operates in deep DCM. With the higher value of R_b, there is a peak in efficiency while with the lower R_b, the curve is strictly monotonic. The waveforms for Modes II and III are shown in Figures 6.23 and 6.24. The Corresponding PWM signals and the currents i_b and i_c are shown in each mode, confirming the theoretical analysis and simulations.

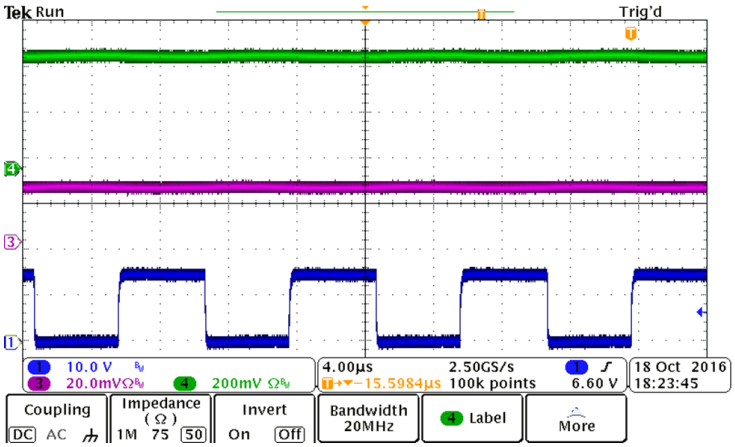

Figure 6.17: near zero-ripple currents at PV and battery ports

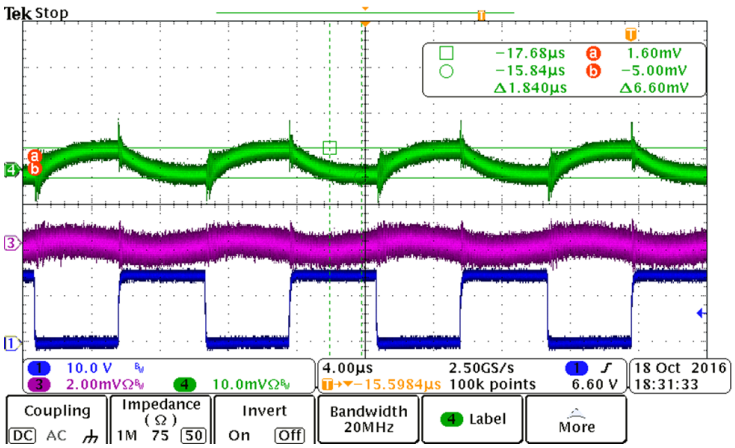

Figure 6.18: ac ripple in i_b : 10 A/V

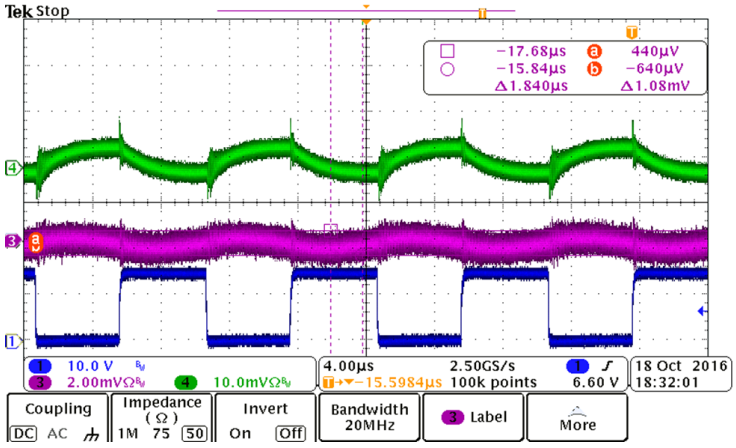

Figure 6.19: ac ripple in i_{pv} : 100 A/V

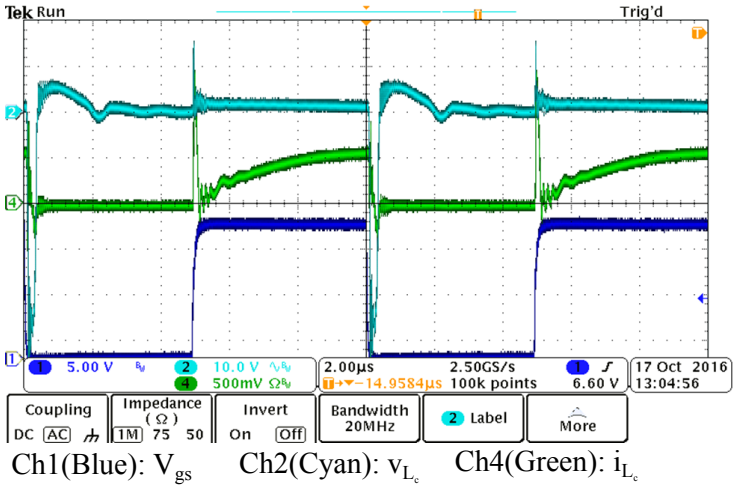

Figure 6.20: DCM port inductor waveforms

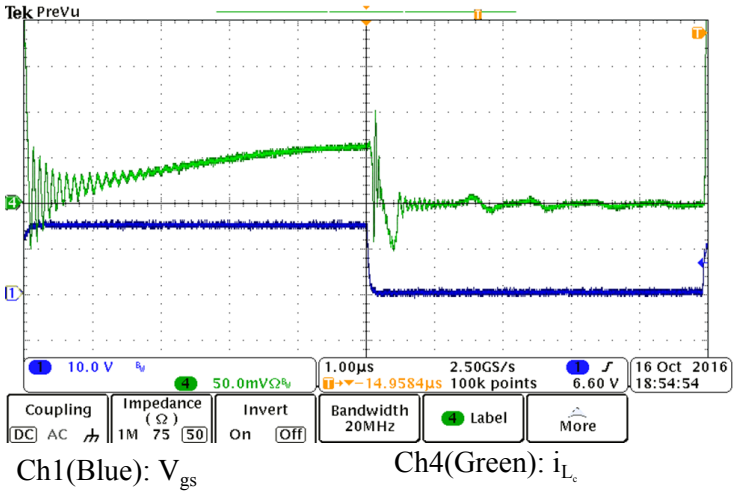

Figure 6.21: Zoomed version of the inductor current showing the DCM entry and parasitic ringing

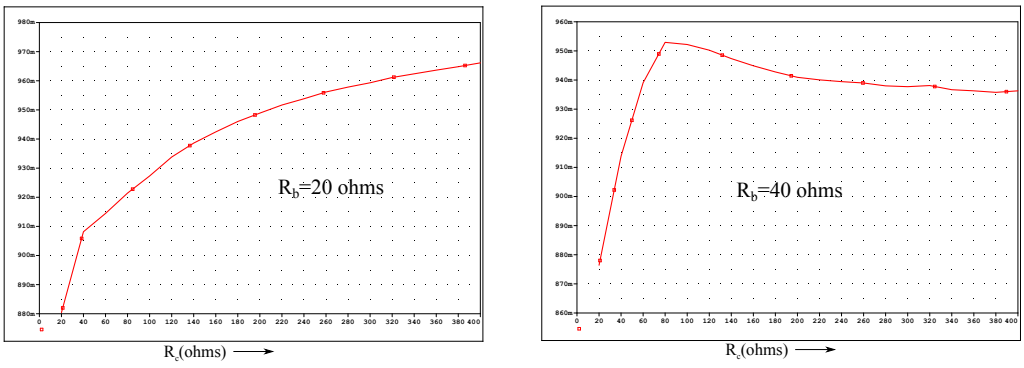

Figure 6.22: Efficiency Plots

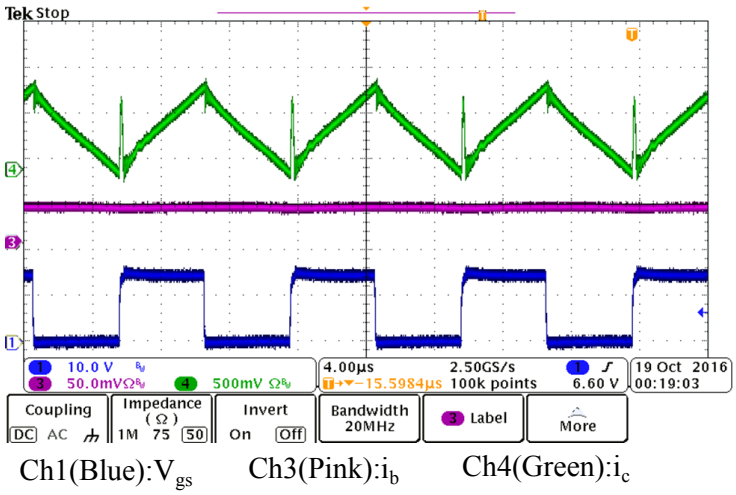

Figure 6.23: Waveforms for Mode II

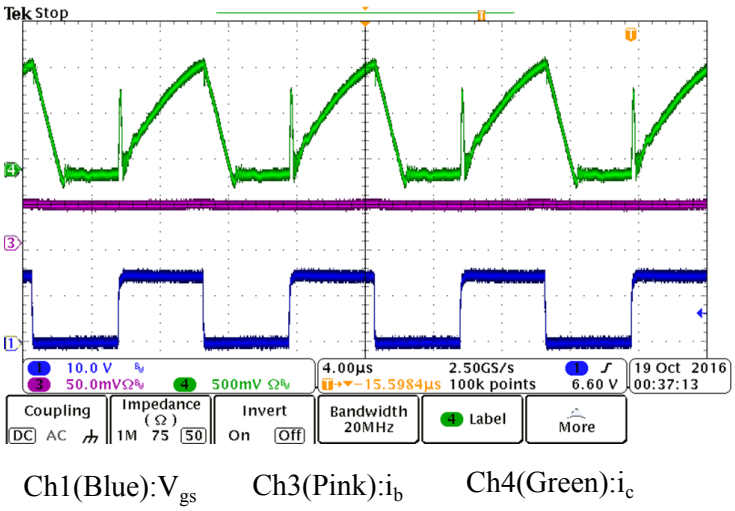

Figure 6.24: Waveforms for Mode III

Chapter 7

Other Hybrid High Step-up Transformerless Topologies

7.1 Introduction

With the advent of wide band-gap devices [64], highly compact low-profile dc-dc converters are becoming an exciting new research area in power electronics. So far, these converters have been able to penetrate applications like Light Detection and Ranging (LiDaR), point-of-load, Class D Audio and in some cases, wireless power [65]. Availability of superior semiconductor materials such as Gallium Nitride has pushed the switching frequencies of non-isolated dc-dc converters upto tens of MHz, as demonstrated in [66].

However, all advances in semiconductor technology are not very useful if limited by parasitics in passive devices. This is exactly what happens in isolated dc-dc converters requiring transformer isolation, such as in PV-to-grid applications [31, 32]. The high step-up ratio requires a large number of primary and secondary layers on the isolation transformer. Usually these layers are interleaved to reduce proximity losses, which can otherwise become significant [29]. The interleaving causes an increase in interwinding capacitance, and ultimately limits the switching frequency of the converter to usually around 100-200 kHz , beyond which the transformer starts to exhibit capacitive behavior [67].

The way around it is to propose non-conventional power electronics topologies, which borrow some ideas from low power circuits such as switch-capacitor dc-dc converters.

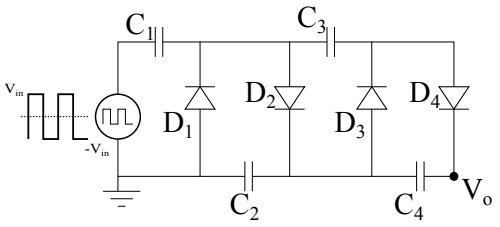

Figure 7.1: 4-stage Cascade Multiplier

The rest of this chapter focuses on a couple of disruptive topological innovations. Section 7.2 gives a brief introduction to the villard cascade voltage multiplier circuit [68]. Section 7.3 talks about the proposed half-bridge and full-bridge diode-capacitor Ćuk converters and their operation principles. Section 7.4 compares the proposed topologies with Middlebrook's topology [30].

7.2 A Brief Recap of the Villard Cascade Multiplier Circuit

The basic voltage multiplier circuit is shown in Fig. 7.1. The basic stages in the build up of the output voltage V_o are shown in Fig. 7.2. It requires four cycles of operation of the square pulse voltage waveform at input (with amplitude V_{in}) to achieve a steady dc voltage of $V_o = 4V_{in}$.

The transient buildup of V_o is described as follows.

1. negative input ($-V_{in}$): The C_1 capacitor is charged through diode D_1 to V_{in} (potential difference between left and right plate of the capacitor is V_{in})

2. positive input (V_{in}): the potential of C_1 adds with that of the source, thus charging C_2 to $2V_{in}$ through D_2.

3. negative input: potential of C_1 has dropped to 0 V thus allowing C_3 to be charged through D_3 to $2V_{in}$.

4. positive input: potential of C_2 rises to $2V_{in}$ (analogously to step 2), also charging C4 to $2V_{in}$. The output voltage (the sum of voltages under C_2 and C_4) rises until $4V_{in}$ is reached.

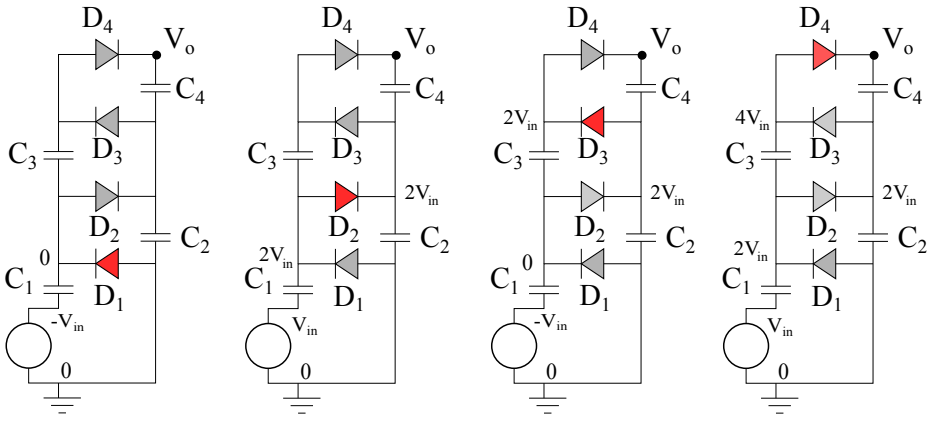

Figure 7.2: Transient Buildup of Output Node Voltage

Hence a high-step up ac-to-dc conversion is achieved without the use of transformer isolation. We use the same concept in the following sections and combine it with a PWM feature in order to achieve the voltage conversion ratio of an isolated Ćuk converter, which is $\frac{nD}{1-D}$.

7.3 The Half-Bridge Flying Capacitor Ćuk Topology

A notable issue with charge-pump circuits is the voltage droop due to loading at output, which is an inherent feature of the converter and cannot be corrected by closed-loop control [69].

The topology and the requisite PWM pulses are shown in Fig. 7.3 and Fig. 7.4 respectively. The features of the topology can be broken into sub-parts:

1. The basic Ćuk converter consisting of inductors L_{pv}, L_g, L_M, energy transfer capacitors C_a, C_b and the PWM switches S_1 and S_2. In the original Ćuk converter, S_1 and S_2 would be combined into a single switch S.

2. The 4-stage diode-capacitor ladder consisting of D_1 to D_4 and C_1 to C_4.

3. The half-bridge voltage balancing capacitors C_{hb1} and C_{hb2}, and the corresponding switches S_{hb1} and S_{hb2}, which are complementary PWM signals with 50% duty-ratio at the input of the diode-capacitor ladder.

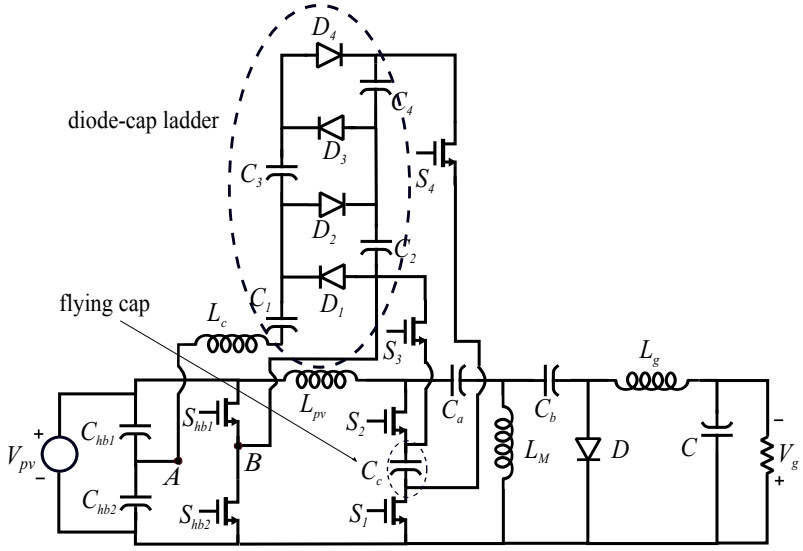

Figure 7.3: Half-Bridge Flying Capacitor Ćuk Topology

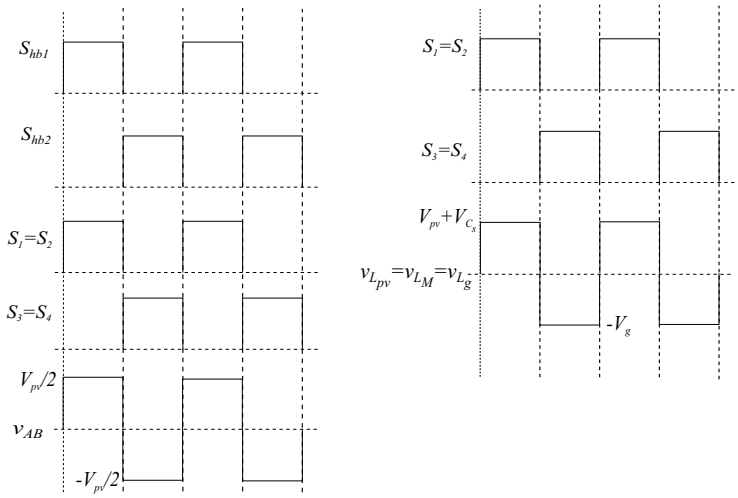

Figure 7.4: PWM waveforms

4. The flying capacitor C_s which generates an extra volt-second balance term during one PWM interval so as to generate the desired conversion ratio of $\frac{nD}{2(1-D)}$. This will become clear in the next section.

5. The proportional voltage waveform across the magnetic windings is still maintained from the original Ćuk converter, which means that an integrated magnetic version of the converter can be developed.

Converter Operation and Voltage Conversion Ratio

The half-bridge circuit consisting of C_a, C_b, S_1 and S_2 generate a symmetrical bidirectional square wave V_{AB} as shown in Fig. 7.4. This square wave is fed to the input of the diode-capacitor ladder circuit (in this case a 4-stage one) as shown in Section 7.2. This actually charges the flying capacitor C_s to a value $4 * V_{pv}/2 = 2V_{pv}$. This charge is replenished during the S_1 low interval while it is depleted to some extent during S_1 high interval. The steady-state dc conversion ratio is derived by volt-second balance across L_{pv}. This gives

$$< v_{L_{pv}} >= 0 \implies D(V_{pv} + V_{C_s}) + (1 - D)(-V_g) = 0 \tag{7.1}$$

Since $V_{C_s} = 2V_{pv}$,

$$\frac{V_g}{V_{pv}} = \frac{3D}{1 - D} \tag{7.2}$$

For a n-stage diode capacitor ladder, we have

$$\frac{V_g}{V_{pv}} = \frac{(\frac{n}{2} + 1)D}{1 - D} \tag{7.3}$$

7.4 The Full-Bridge Flying Capacitor Ćuk Topology

The topology and the requisite PWM pulses are shown in Fig. 7.5 and Fig. 7.6 respectively. The features of the topology are exactly the same as in the half-bridge case, except that the half-bridge generation circuit is replaced by a full-bridge topology. Again, the proportional voltage waveform across the magnetic windings is still maintained from the original Ćuk converter, which means that an integrated magnetic version of the converter can be developed.

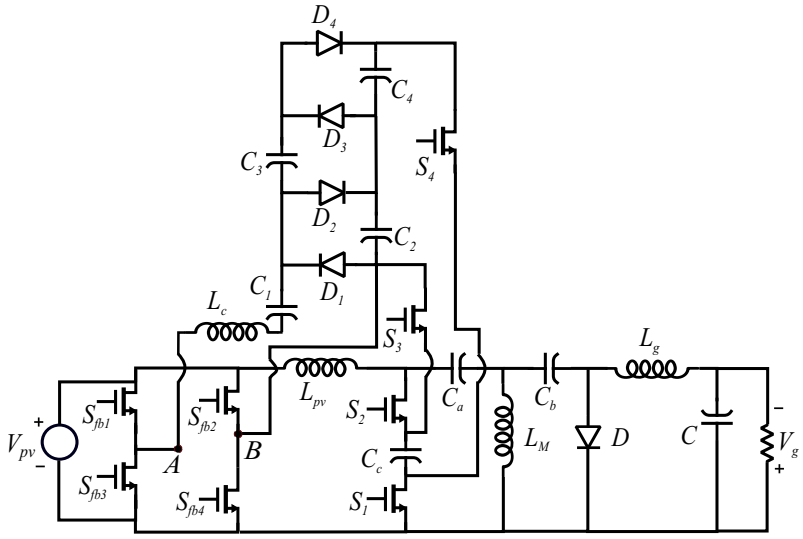

Figure 7.5: Full-Bridge Flying Capacitor Ćuk Topology

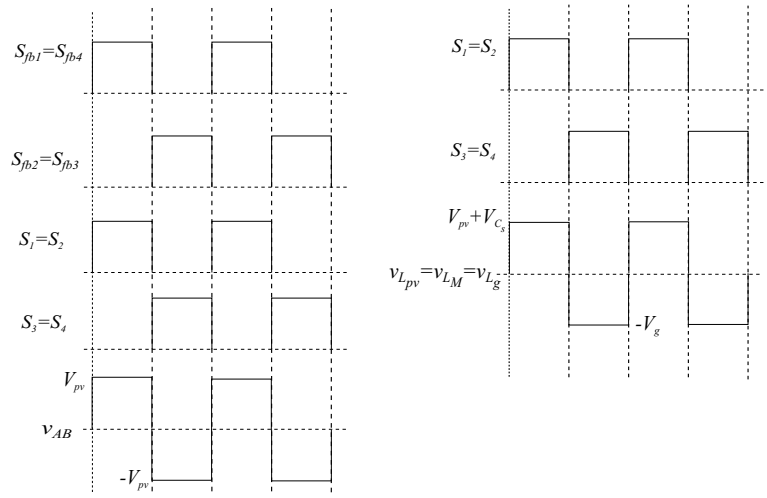

Figure 7.6: PWM waveforms

Table 7.1: Specifications

Parameter	Value
$L_{pv} = L_M = L_g$	500 μH
$C_a = C_b = C$	100 μF
f_S	100 kHz
C_s	200 μF
$C_1 = C_2 = C_3 = C_4$	200 μF
V_{pv}	30V
n	4
R	50 Ω

Converter Operation and Voltage Conversion Ratio

The full-bridge circuit consisting of switches $S_{fb1} - S_{fb4}$ generate a symmetrical bidirectional square wave V_{AB} as shown in Fig. 7.6. This square wave is fed to the input of the diode-capacitor ladder circuit (in this case a 4-stage one) as shown in Section 7.2. This actually charges the flying capacitor C_s to a value $4V_{pv}$. This charge is replenished during the S_1 low interval while it is depleted to some extent during S_1 high interval. The steady-state dc conversion ratio is derived by volt-second balance across L_{pv}. This gives

$$< v_{L_{pv}} >= 0 \implies D(V_{pv} + V_{C_s}) + (1 - D)(-V_g) = 0 \tag{7.4}$$

Since $V_{C_s} = 4V_{pv}$,

$$\frac{V_g}{V_{pv}} = \frac{5D}{1 - D} \tag{7.5}$$

For a n-stage diode capacitor ladder, we have

$$\frac{V_g}{V_{pv}} = \frac{(n+1)D}{1 - D} \tag{7.6}$$

7.5 Simulation Results

The simulation results for a full-bridge converter with the simulation parameters enlisted in Table I are shown next in Fig. 7.7:

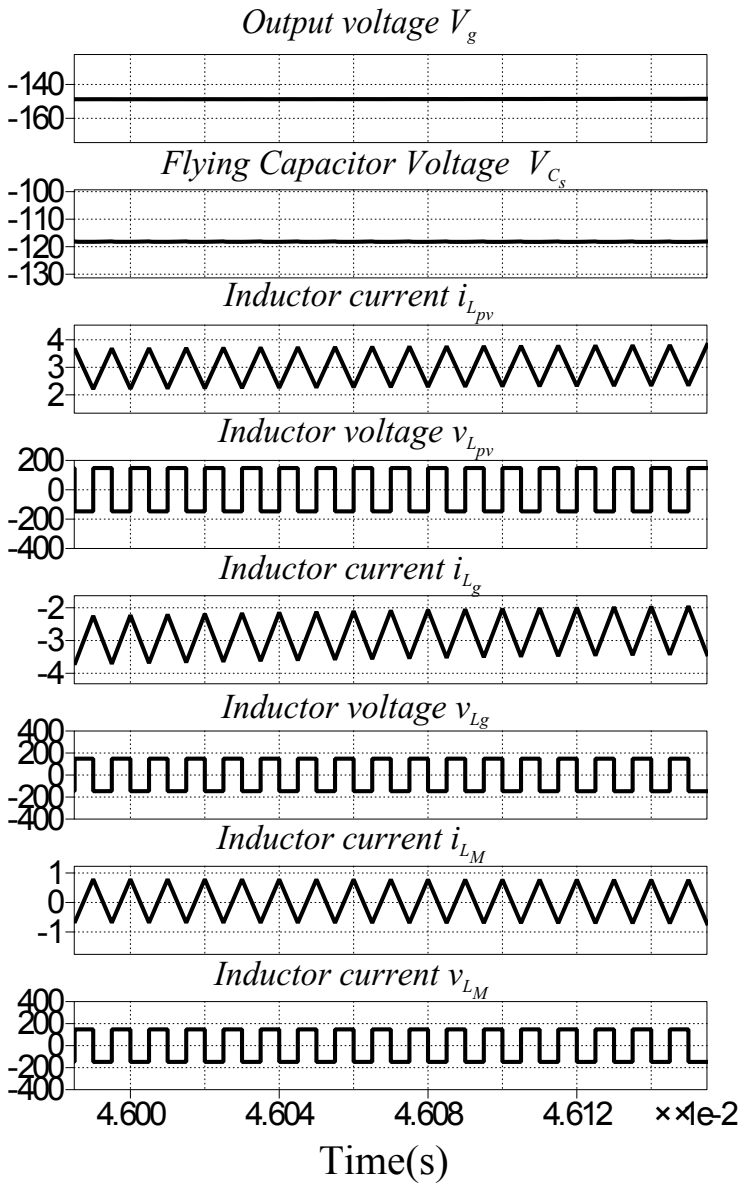

Figure 7.7: Waveforms for the Full-Bridge Flying Capacitor Ćuk converter

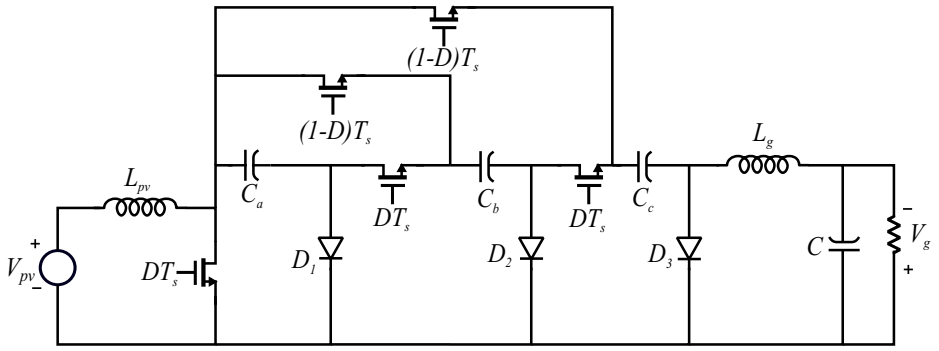

Figure 7.8: High Step-up Transformerless Ćuk converter proposed by Middlebrook [30]

7.6 Comparison with Middlebrook's Topology

The Ćuk converter is unique compared with the conventional buck, flyback and other converters in that it utilizes capacitive rather than magnetic energy transfer. It is this property that permits the capacitance voltage divider feature to be incorporated. The circuit, shown in Fig. 7.8, is a "voltage step-up" Ćuk converter in which the energy transfer capacitors C_a, C_b and C_c are charged in parallel and discharged in series. Each extra capacitor requires two extra transistors and one extra diode. For N energy transfer capacitors, the voltage conversion ratio is given by

$$\frac{V_g}{V_{pv}} = \frac{ND}{1-D} \tag{7.7}$$

A preliminary comparison between the two topologies proposed in this chapter and Middlebrook's topology are shown in Table 7.2 for the same voltage conversion ratio. For convenience, we will denote Middlebrook's topology as T_M, the proposed half bridge topology as T_{hb} and the proposed full bridge topology as T_{fb}. It is evident that for higher step-up, i.e., $n > 3$ the half-bridge wins in terms of switch count. The full-bridge has two extra switches , however, it has two less bulky energy storage capacitors and no voltage-balancing issues to deal with. Plus, full-bridge semiconductor modules are readily available on the market, making it a more easier converter to implement.

However, this is only a very preliminary comparison and switch current and voltage stresses need to be investigated in the circuit. Another factor is that the PV panel

Table 7.2: Comparison

	T_M	T_{hb}	T_{fb}
Transistors	2n	6	8
Diodes	n	n	n

needs to, atleast, periodically supply large currents to charge the capacitors $C_1 - C_4$. According to the topology, there is no inherent current limiting mechanism. This is usually not a problem for signal processing circuits where such topologies are normally used. A resonant charging inductor L_c is inserted into the circuits 7.4 and 7.5 in order to control this charging current. The desing of the indcutor is a tradeoff which needs to be investigated in order to make the case for these topologies. Nevertheless, it makes an exciting new area of research.

Chapter 8

Conclusion and Future Work

Multi-port Converters are becoming extremely popular in recent literature for their applications in renewable energy power distribution. This can be attributed to their plug and play capability, and being able to interface widely nominal voltages. However the onus is to reduce the part count and integrate the components as much as possible, without sacrificing the power quality, reliability or efficiency.This thesis addresses this need by arguing the case for variants of the Ćuk Converter as a promising topology in this regard. All the topologies have the advantage of a completely or atleast partially integrated magnetic structure, which reduces part count, improves efficiency and have enhanced performance in terms of emulating a perfect DC-DC transformer, which is the principal goal of a switched-mode converter. Although the converter promises some very exotic features, it also brings with it unforeseen complexity of designing the magnetics. This thesis proposes two methods derived from the area-product and geometrical constant, which are completely analytical and are, for the first time, ready-to-be-adopted methods in industry for the design of these zero-fundamental-ripple integrated magnetic converters. This thesis also proposes three novel topologies, exploring the utilization of DCM and hybrid flying capacitor topologies which further expedite the adoption of this extremely intriguing power converter topology.

8.1 Conclusion

Chapter 2 introduces the concept of magnetic integration and discusses the advantages of having such a structure. The basic idea for this integration lies behind the fact

that windings with proportional voltage waveforms can be coupled onto a single magnetic structure. This is actually the reversal of the cause-and-effect in a two-winding transformer. The idea can obviously be extended to three windings. This idea is demonstrated in the basic Ćuk topology. The magnetic scaling law quantitatively demonstrates the advantages to be gained in power density of such a structure. We also delve deeper to find that an improvement in performance can also be obtained in terms of zero-ripple terminal currents, apart from the gain in power density. However, although the circuit equations (inductance matrix model) can be solved to yield a condition, it does not say much about the actual design.

With the conclusions of Chapter 2, Chapter 3 explains a ready-to-implement area product approach for a two-port integrated magnetic Ćuk Converter while still adhering to the circuit equations. The type of core, inductance matrix requirement for zero-ripple, saturation flux density, finite-element-modelling, window area are all taken into account to provide a comprehensive analytical procedure for a range of duty-ratio and other specifications catered to a PV-to-battery application. The results of FEA and Pspice simulations have proved the method to be accurate and hardware ready. The zero-ripple condition has been verified with sufficient accuracy in hardware. An investigation into the efficiency of this converter, as well as the relevant passive snubber and thermal design has also been discussed.

In chapter 4, we deal with a different method of designing the integrated magnetics, but for the same application. The method takes into account peak flux density, peak-to-peak ripple in the magnetizing inductance and also optimizes the copper loss. The results of FEA and Pspice simulations have proved the method to be accurate and hardware ready. Hardware design should be fairly straightforward from this point. Future work entails generalizing the design for bidirectional power flow (for battery etc.), as well as for a PV-to-battery application.The design method can also be upgraded based on optimizing the copper as well as core loss of the converter including proximity effects. This will utilize the K_{gfe} approach [29, 49]. Additionally, the method can be compared against traditional methods such as the area product.

Even with this performance improvement, it remains to be seen whether further efficiency improvements can be added, especially by soft-switching. In Chapter 5 such a scheme is explained, for a three-port integrated magnetic topology. A similar scheme had already been discussed in [63, 71] for a two-port version of this converter. This chapter extends the same work to three ports. Some new components are added, an

extra switch and clamp capacitor to achieve ZVS turn-on of the switches. Also a high-frequency resonant snubber branch is added for achieving close to ZCS turn-off of the switches. All these reduce switch voltage stresses. However, there is also an inherent loss of symmetry in the converter structure once the components are added. This affects the "proportional voltage waveform" requirement for the zero-ripple while adding efficiency enhancement. This tradeoff is the investigation of the simulation in this chapter.

In chapter 6, we move away to a different direction so as to add some more useful features to the three-port Ćuk converter instead of single-mindedly focusing on the magnetics design. A modified version of a three-port Ćuk converter has been proposed for interfacing PVs with battery storage and a supercapacitor port which forms part of dc-bus for a microinverter architecture. The converter possesses the highly desirable zero fundamental ripple current property on two of its ports (PV and battery) of our earlier work [18] while it also investigates a combined CCM-DCM operation in order to interface with a grid-tied inverter. Additionally, it is also demonstrated how to operate this converter with just two active ports (supercapacitor and battery) for bidirectional power flow. The magnetics design of the three-winding coupled inductor is crucial and is descirbed in depth. Finite Element Modelling and Analytical Area-Product Methods are used to design this integrated inductor. The operation of the converter in steady-state is confirmed by means of simulation and experimental results. The experimental efficiency of this converter in various modes is also dealt with.

The penultimate chapter of this thesis, Chapter 7, deals with some disruptive innovations in power converter circuit topologies to bring the blessings of wide band-gap devices and planar magnetics to multi-port power conversion for renewables to interface with grid and storage. A couple of topologies are proposed which utilize some diode-capacitor circuits to achieve a high step-up while still maintaining the basic properties of PWM Ćuk converters. Simulation results are shown which confirm these. These topologies are compared with a topology structure proposed by Middlebrook [30] which show that our topologies have a lower switch count, especially for high step-up PV applications.

8.2 Future Work

There is a plethora of future research incentives for such a topology. More specifically, these are:

- Isolated version of the three-port non-isolated Ćuk converter proposed in Chapter 6. Hardware results for the same.
- Using the K_{gfe} method to design the magnetics.
- Investigation of combinations of the two inductor topologies, Sepic, Ćuk and Zeta. This means one of the three-ports can be a Sepic or Zeta port, depending on the load requirement. Then all the topologies need to be evaluated against standard benchmarks of efficiency and EMI.
- Hardware validation of the topologies proposed in Chapter 7.
- Switched-capacitor versions of the converter topologies proposed in Chapter 7. This means that the factor n can be reconfigurable, leading to an elegant high step-up converter with the use of wide band-gap semiconductor technology.
- Dynamic small-signal modelling and power management for the three-port converter. A prominent paper in this regard is [70].
- Investigation into a four-port extension of such a converter. Probably requires a unique magnetic structure and the extra-port can be incorporated into the circuit by means of Middlebrook's extra-element theorem.

Chapter 9

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Appendix A

Derivation of peak flux densities $\hat{B}_2$, $\hat{B}_1$ and $\hat{B}$:

Since i_{pv} and i_g are purely dc, the peak quantities of ϕ_2, ϕ_1 and ϕ can be written as:

$$\hat{\phi_2} = \frac{1.5N_gI_g - 0.5N_{pv}I_{pv}}{\mathcal{R}} + \frac{max(N_pi_p + N_si_s)}{\mathcal{R}} \tag{A.1}$$

$$\hat{\phi_1} = \frac{1.5N_{pv}I_{pv} - 0.5N_gI_g}{\mathcal{R}} + \frac{max(N_pi_p + N_si_s)}{\mathcal{R}} \tag{A.2}$$

$$\hat{\phi} = \frac{N_{pv}I_{pv} + N_gI_g}{\mathcal{R}} + \frac{2 * max(N_pi_p + N_si_s)}{\mathcal{R}} \tag{A.3}$$

Using $V_gI_g = V_{pv}I_{pv}$ and $n = \frac{V_g(1-D)}{V_{pv}D}$, we have the following set of equations:

$$1.5N_gI_g - 0.5N_{pv}I_{pv} = N_{pv}I_{pv}\left(\frac{2(1.5-2D)}{D}\right) \tag{A.4}$$

$$1.5N_{pv}I_{pv} - 0.5N_gI_g = N_{pv}I_{pv}\left(2 - \frac{0.5}{D}\right) \tag{A.5}$$

$$N_{pv}I_{pv} + N_gI_g = N_{pv}I_{pv}\left(\frac{1}{D}\right) \tag{A.6}$$

Replacing the first terms in (A.1)-(A.3) using (A.4)-(A.6), we have

$$\hat{B_2} = \frac{2\hat{\phi_2}}{A_c} = \frac{N_{pv} I_{pv} f_{\phi_2}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R} A_c}$$
$$\hat{B_1} = \frac{2\hat{\phi_1}}{A_c} = \frac{N_{pv} I_{pv} f_{\phi_1}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R} A_c}$$
$$\hat{B} = \frac{\hat{\phi}}{A_c} = \frac{N_{pv} I_{pv} f_{\phi}(D) + 2 * max(N_p i_p + N_s i_s)}{\mathcal{R} A_c}$$

where

$$f_{\phi_2}(D) = \frac{2(1.5 - 2D)}{D} \tag{A.7}$$
$$f_{\phi_1}(D) = 2\left(2 - \frac{0.5}{D}\right) \tag{A.8}$$
$$f_{\phi}(D) = \frac{1}{D} \tag{A.9}$$

Appendix B

Expression for Magnetizing Inductance

From Fig. 3, the exact expression for the magnetizing inductance of the isolation transformer, or the self-inductance of the transformer primary winding, is given by

$$L_p = \frac{N_p^2}{\mathcal{R}_g + \mathcal{R}_m} \tag{B.1}$$

where $\mathcal{R}_g$ and $\mathcal{R}_m$ are the reluctances due to the air-gap and ferrite core respectively. They are defined as follows:

$$\mathcal{R}_g = \frac{x/4}{\mu_0 A_c}, \quad \mathcal{R}_m = \frac{l_m}{\mu_0 \mu_r A_c} \tag{B.2}$$

Equation (34) is valid when the reluctance contribution from the ferrite core is negligible. In other words, this is true when

$$\mathcal{R}_g > 10\mathcal{R}_m \implies \frac{x}{2} > \frac{10 l_m}{\mu_r} \tag{B.3}$$

Appendix C

Derivation of $i_{p,rms}$ and $i_{s,rms}$:

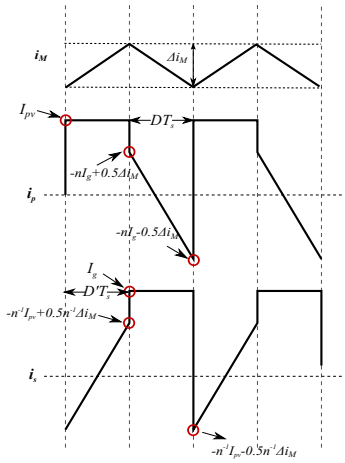

Figure C.1: Transformer Primary, Secondary and Magnetizing (referred to primary) Current Waveforms

$$i_{p,rms} = \sqrt{\int_0^{D'T_s} I_{pv}^2 \frac{dt}{T_s} + \int_{D'T_s}^{T_s} \left(-nI_g + \frac{\Delta i_M}{2} - \frac{\Delta i_M t}{DT_s} \right)^2 \frac{dt}{T_s}}$$

$$= \sqrt{T_1 + T_2 + T_3 + T_4} \quad \text{where} \quad \text{(C.1)}$$

$$T_1 = (1-D){I_{pv}}^2 \tag{C.2}$$

$$T_2 = D(0.5\Delta i_M - \frac{(1-D)I_{pv}}{D})^2 \tag{C.3}$$

$$T_3 = \Delta i_M(0.5\Delta i_M - \frac{(1-D)I_{pv}}{D})\frac{2D-D^2}{1-D} \tag{C.4}$$

$$T_4 = {\Delta i_M}^2\frac{3D-D^2+D^3}{3(1-D)^2} \tag{C.5}$$

$$i_{s,rms} = \sqrt{\int_0^{D'T_s}\left(\frac{-I_{pv}}{n} - \frac{\Delta i_M}{2n} + \frac{\Delta i_M t}{DT_s}\right)^2\frac{dt}{T_s} + \int_{D'T_s}^{T_s} I_g^2\frac{dt}{T_s}}$$

$$= \sqrt{T_5+T_6+T_7+T_8} \quad \text{where} \tag{C.6}$$

$$T_5 = \frac{(1-D)^2{I_{pv}}^2}{Dn^2} \tag{C.7}$$

$$T_6 = (1-D)(\frac{I_{pv}}{n} + \frac{\Delta i_M}{2n})^2 \tag{C.8}$$

$$T_7 = \Delta i_M(\frac{I_{pv}}{n} + \frac{\Delta i_M}{2n})\frac{1-D^2}{nD} \tag{C.9}$$

$$T_8 = {\Delta i_M}^2\frac{1-D^3}{3n^2D^2} \tag{C.10}$$

Appendix D

Derivation of peak flux densities $\hat{B}_2$, $\hat{B}_1$ and $\hat{B}$ in non-isolated TPC:

Since i_{pv} and i_b are purely dc, the peak quantities of ϕ_1, ϕ_2 and ϕ can be written as:

$$\hat{\phi_1} = \frac{1.5N_{pv}I_{pv} - 0.5N_bI_b}{\mathcal{R}} + \frac{max(N_M i_M)}{\mathcal{R}} \tag{D.1}$$

$$\hat{\phi_2} = \frac{1.5N_bI_b - 0.5N_{pv}I_{pv}}{\mathcal{R}} + \frac{max(N_M i_M)}{\mathcal{R}} \tag{D.2}$$

$$\hat{\phi} = \frac{N_{pv}I_{pv} + N_gI_g}{\mathcal{R}} + \frac{2 * max(N_M i_M)}{\mathcal{R}} \tag{D.3}$$

Using $N_{pv} = N_b$ and $r_p = \frac{V_bI_b}{V_{pv}I_{pv}}$, we have the following set of equations:

$$1.5N_{pv}I_{pv} - 0.5N_bI_b = N_{pv}I_{pv}\left(1.5 - 0.5r_p\frac{1-D}{D}\right) \tag{D.4}$$

$$1.5N_bI_b - 0.5N_{pv}I_{pv} = N_{pv}I_{pv}\left(1.5r_p\frac{1-D}{D} - 0.5\right) \tag{D.5}$$

$$N_{pv}I_{pv} + N_gI_g = N_{pv}I_{pv}\left(1 + r_p\frac{1-D}{D}\right) \tag{D.6}$$

Replacing the first terms in (D.1)-(D.3) using (D.4)-(D.6), we have

$$\hat{B_1} = \frac{2\hat{\phi_1}}{A_c} = \frac{N_{pv} I_{pv} f_{\phi_1}(D, r_p) + 2 * max(N_M i_M)}{\mathcal{R} A_c}$$

$$\text{where} \quad f_{\phi_1}(D, r_p) = 3 - \frac{(1-D) r_p}{D} \quad \text{(D.7)}$$

$$\hat{B_2} = \frac{2\hat{\phi_2}}{A_c} = \frac{N_{pv} I_{pv} f_{\phi_2}(D, r_p) + 2 * max(N_M i_M)}{\mathcal{R} A_c}$$

$$\text{where} \quad f_{\phi_2}(D, r_p) = \frac{3 r_p (1-D)}{D} - 1 \quad \text{(D.8)}$$

$$\hat{B} = \frac{\hat{\phi}}{A_c} = \frac{N_{pv} I_{pv} f_{\phi}(D, r_p) + 2 * max(N_M i_M)}{\mathcal{R} A_c}$$

$$\text{where} \quad f_{\phi}(D, r_p) = 1 + \frac{r_p (1-D)}{D} \quad \text{(D.9)}$$

Appendix E

Magnetic Circuit Analysis and Derivation of Zero-Ripple Condition:

The spacer air-gap is $x/2$, while the cross-section area is S (Fig.3). We define the following parameters:

$$R = \frac{x}{\mu_0 S/2}, \quad L_m = \frac{N^2}{R} \tag{E.1}$$

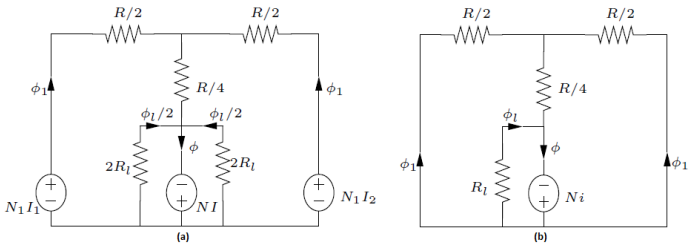

Figure E.1: Effective three-winding structure and zero-ripple circuit

Table E.1: Magnetic Circuit

Parameter	Description
l	leakage parameter
B_m	saturation flux density
L	center leg inductance
S	center-leg cross-section
N	no. of turns of transformer primary
N_1	no. of turns of input inductor winding
I_1	input inductor dc current
I_2	output inductor dc current
I	isolation transformer magnetizing current
$x/2$	spacer air gap

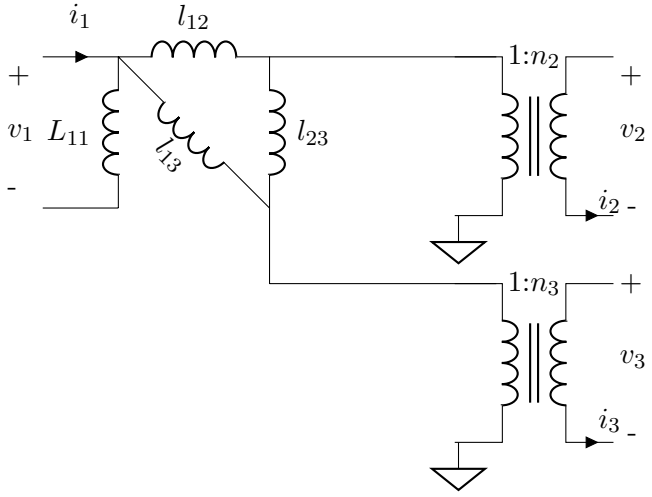

Figure E.2: Three-winding extended cantilever model

E.1 The Dual-Inductance/Cantilever Circuit Model

The merits of the extended cantilever model are discussed in [52]. The extended cantilever model contains the correct number of parameters, $n(n+1)/2$ required to describe a n-winding magnetic structure. The model is completely general in that it can be related to the inductance matrix. It also has the advantage that each parameter in the model can be measured directly by means of open-circuit and short-circuit tests, and that leakage inductances can be found. Such a model of the 3-winding structure is shown in Fig.5. The parameters can be measured using a network analyzer without performing ill-conditioned numerical computations. Winding 1 is the center winding, while Windings 2 and 3 are the ones on the outer legs.

Open-Circuit Test:

$$n_1 = 1, n_2 = \frac{v_2}{v_1}, n_3 = \frac{v_3}{v_1} \tag{E.2}$$

where

v_1 = voltage applied across winding 1

v_2 = open-circuit voltage across winding 2, and

v_3 = open-circuit voltage across winding 3.

Short-Circuit Test:

l_{12}, l_{23}, l_{13} are the leakage inductances described in Fig.5. Each l_{ij} is measured by a short circuit test, i.e., driving the ith winding with an ac voltage source and measuring the short circuit current on the jth winding with the appropriate phase considerations [52].

$$l_{ij} = \frac{1}{s}\frac{1}{n_i n_j}\frac{v_i(s)}{i_j(s)} \tag{E.3}$$

Apart from these, we have

$$l_2 = n_2^2(l_{12} \| l_{23}), l_3 = n_3^2(l_{13} \| l_{23}) \tag{E.4}$$

which are the Thevenin inductances seen at Ports 2 and 3 (Fig.5).

Now the ripple across winding j is given by $\Delta i_j \propto (1 - \alpha_j)$, where $j = 2, 3$. [15]

where

$$\alpha_2 = \frac{l_2}{n_2 l_{12}} + \frac{l_2}{n_3 l_{23}} \tag{E.5}$$

$$\alpha_3 = \frac{l_3}{n_3 l_{13}} + \frac{l_3}{n_3 l_{23}} \tag{E.6}$$

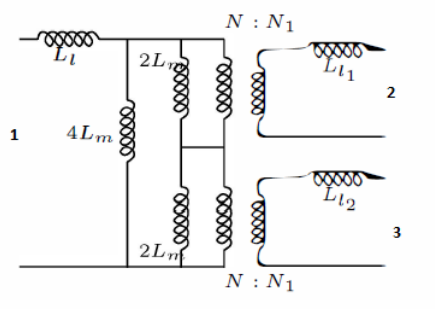

Figure E.3: Dual Inductance Model

The dual-inductance model (Fig. E.3) is obtained by a duality transformation from the flux-reluctance (physical) model shown in Fig.4(a)[45]. Comparing the cantilever model (Fig. E.2) with the dual inductance model(Fig. E.3), we have

$$l_{12} = l_{13} = \frac{L_l(4L_m + L_l)}{2L_m} \tag{E.7}$$

$$l_{23} = 2l_{12} \tag{E.8}$$

$$n_2 = n_3 = \frac{N_1}{N}.\frac{2L_m}{4L_m + L_l} \tag{E.9}$$

Substitute l_{12}, l_{13} from (17)-(20) into (14)-(16). Then equating $\alpha_2 = \alpha_3 = 1$ provides zero-ripple currents at Terminals 2 and 3. This yields

$$n_2 = n_3 = 1 \Longrightarrow \frac{N_1}{N} = 2 + \frac{x}{l} \tag{E.10}$$

Note that this is equivalent to setting the voltage across the outer winding leakage inductances L_{l_1} and L_{l_2} to zero in Fig. E.3.